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A Modified Design of Luo DC-DC Converter Based-on Multi-Switched Capacitor Cell Technique

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By

Asmaa Aqeel Hadi Mahdi

Under Supervision of

Prof .Dr. Hassan Jassim Motlak

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بسم الله الرحمن الرحيم

صدق الله العلي العظيم

المجادلة :11

Supervisors Certification

I certify that this thesis titled **"Design and Simulation of Luo DC-DC converter Based-on Multi-Switched Capacitor Cell Technique"** was prepared by **Asmaa Aqeel Hadi Mahdi** under my supervision at the Electrical Engineering Department, College of Engineering at the University of Babylon, in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering/Electronics.

Supervisor

Signature:

Name*: Prof. Dr. Hassan Jassim Motlak*

Date: / / 2024

Given the available recommendation, we forward this thesis for debate by the examining committee.

Head of the Electrical Engineering Department

Signature:

Name: *Prof. Dr. Qais Kareem Omran*

Date: / / 2024

Abstract

Fossil fuels like coal, gas, and oil are efficient but cause pollution and are limited. As a result, more focus is on solar energy, like solar-powered cars and battery storage. However, these systems produce direct current (DC) electricity, which makes connecting to the power grid more challenging.

This work presents the modified design of the DC-DC positive output super lift Luo converter (POSLLC) circuit by adding a switched capacitor (SC) cell . It was designed and analyzed then compared with conventional positive output super lift Luo converter to show the enhancement in the performance of the modified circuit. A multi-switched capacitor was connected at the output stage of the proposed system. The SC cell improves the dependability and lifespan of the source and maintains the input voltage. It is also provides more voltage amplification, particularly for high-gain purposes utilizing a single power switch.

A conventional POSLLC circuit was constructed and simulated using MATLAB/SIMULINK with a duty cycle of 0.5 and input voltage was set 12 VDC, resulting in an output voltage of 36 volts , a voltage gain of three times the input voltage. Then the proposed modified POSLLC circuit was designed by including a switched capacitor cell, achieving at a duty cycle of 0.5, an output voltage of 60 volts, a voltage gain of five times the input voltage. Moreover, A multi-switched capacitor cell was then incorporated into the circuit at a duty cycle of 0.5, resulting in an output voltage of 240 volts and a voltage gain of 20 times the input voltage.

The proposed converter effectively achieves significant voltage enhancements with superior performance characteristics, as validated by the outcomes of theoretical analysis, circuit design, and simulations. Further investigation into high-gain power conversion systems is facilitated by findings indicating that the multi-switched capacitor approach is an appropriate technique for enhancing the voltage gain of POSLLC.

Table of Content

List of Symbols and Abbreviations	
AC	Alternate Current
C	Capacitor
CCM	Continuous Conduction Mode
CP	Charge Pump
Co	Output Capacitor
DC	Direct Current
DCM	Discontinuous Conduction Mode
Fs	Switching Frequency
G	Gain
I_{ref}	Reference Current
K	Duty cycle
Ki	Gain in Proportional–Integral Controller Unit
KP	Proportional Gain in Controller Unit
KW	Kilowatt
LED	Light Emitting Diode
MPPT	Maximum Power Point Tracking
MSCC	Multi-Switched Capacitor Cell
MPPT	Maximum Power Point Tracking
NOSLLC	Negative Output Super-Lift LUO Converter
P&O	Perturb and Observe
PI	Proportional–Integral Controller
Pin	Input Power

Po	Output Power
POLC	Positive Output LUO Converter
R	Load Resistance, Ω
R E S	Renewable Energy Sources
S	Switch
S.C	Switched Capacitor
SL	Switched Inductor
T	Total Period
V	Volt
V_{in}	Input Voltage
V_{ref}	Reference Voltage
V_L	Inductor Voltage
V_C	Capacitor Voltage
VL	Voltage Lift
V_O	Output Voltage
ϵ_{CO}	Ripple of Output Capacitor
ζL	Variation Ripple of Inductor Current
Δi	Change in Current
Δ_{IL}	Change In The Inductor Current
Δt	Change in Time

List of Figures

List of Tables		
Table	**Title**	**Page**
Table (1-1)	Performance parameters of POSLC converter	8
Table (2-1)	Types of Topologies	16
Table (2-2)	Comparison for the types of CD-DC Converter	21
Table (2-3)	Comparison between the positive output super- lift Luo converter and some basic boost converters	33
Table (3-1)	The Parameters of Conventional Circuit	40
Table (3-2)	The parameters proposed modified single cell Circuit Parameters	54
Table (3-3)	The parameters of proposed modified multi Switched Capacitor Cell Circuit	58
Table (4-1)	Summarized the simulation results of proposed POSLLC	74
Table (4-2)	Comparison of proposed and other boost converters	75
Table (4-3)	Comparison between the Proposed Converter and DC- DC Converters	76

CHAPTER ONE

Chapter One

Introduction

1.1 Introduction

In recent years, many applications need the range step-up DC-DC converters such as an electric vehicle, medical equipment, servo motor drives, industrial applications, portable devices (e.g. portable computer and mobile phones), internet services and Renewable Energy Sources (RES) (e.g solar energy, fuel cell and wind turbine generator system). One of the most critical issues of using solar energy is variable output energy and low output voltage due to depending on sunlight [1].

In order to avoid this limitation, step-up DC-DC converters have been used. However simple construction and control, straightforward design and operational analysis, and high gain ratio remain difficulties for DC-DC converters [2].

In many power conversion applications, step-up DC-DC converters boost DC power. Using active or passive power switching devices, inductors or capacitors may store energy[3]. DC-DC converters classified into isolated and isolated DC-DC converters. Non-isolated converters, like boost converters enhance voltage by raising duty ratio. Different DC-DC non-isolated converter topologies increase voltage amplification and efficiency. Some applications employ isolated converters for safety, galvanic isolation, and noise resistance.[4]

Simple step-up DC-DC converters include boost, buck-boost, SEPIC, Cuk, and ZETA. Output gain voltage increases with duty cycle [5].For large DC increase, the basic boost duty cycle must exceed 0.8, High duty cycles may cause simple boost recovery diode difficulties [6]. DC/DC boost circuits are essential for many power electronics applications [7].

The alternative available solutions to reach large DC gain, high switching frequency, transformer or coupled inductor with positive and negative converters are used, such as positive super lift Luo converter and negative super lift Luo converter. However these solutions would not be an exact solution due to losses of leakage inductances, cost and sizing, EMI problem, high voltage stress and reducing efficiency. Another solution that uses a cascade of the boost converter (quadratic converters) is widely proposed. However, the overall performance and efficiency of the cascade converter depends on the product of each stage which implies the attracting losses of energy.[8]

Switching capacitors and inductors have large dc gain ratios when charged in parallel and discharged in series [4]. Small switching capacitor cells have merely a capacitor and diode. The output voltage of a switching capacitor converter is determined by the number of capacitors[9]. Poor voltage regulation inhibits switching capacitor converters from transmitting full capacitor capacity to the load, lowering efficiency [4,9].

Also, increasing numbers of capacitor needs more switching device which means more losses. Regarding inductor, the cell can provide increasing in the gain ratio. However, main issues of the inductor cell are cost and sizing. Recently, in order to achieve advanced topology with high efficiency and high power density, the Voltage Lift (VL) converters have been proposed [6,10]. These converters are combining from switched capacitor cell and switched inductor cell. The key problem of VL converter is using more inductor and capacitor as inner storage elements. Luo converters' ease of use and control have made them popular. Positive/negative superlift Luo converters are popular in renewable energy and electric car applications due to their high gain ratio and output voltage flexibility. This family contains basic, relift, and triple circuits.

1.2. Literature Survey

The development of high-voltage step-up DC-DC converter technology is driven by energy efficiency, power density, cost, complexity, and reliability. These factors interact differently. The characteristics and purposes of voltage boosting techniques differ. Many industries and applications need converter topology and control, which were previously difficult and unprofitable. Many combinations of varied and frequently linked voltage-boosting technologies will meet and raise application efficiency [1].

Hsieh YP et. al., 2012[23]: introduced a coupled-inductor, switched-capacitor high-step-up dc to dc converter. Inductors charge and discharge paralleled capacitors in sequence, building on the resultant capacitor. Thus, the proposed converter has high step-up voltage gain and suitable duty ratio. Limit main switch voltage surge. Low principal switching on-state impedance RDS(ON) may minimize conduction loss.

Luo FL, Ye H., 2013 [24]: proposed a super lift (SL) technique using split capacitors and inductors to increase output voltage. It effectively increases power and voltage transfer gain..

Bahrami H. et. al., 2015 [25]: proposed a modified efficient step-up boost converter. It achieves significant voltage gain using coupled-inductor and super-lift methods. Super-lift stage absorbs energy from connected inductor leakage inductance, clamps main switch off-state voltage, and achieves modest voltage gain. The coupled-inductor approach also improves output diode reverse recovery, main switch off-state voltage, and voltage gain. This converter produces significant step-up voltage gain and avoids the disadvantages of the typical boost converter utilizing these two methods.

Rabeb Abid, et. al., 2017 [26]: designed and simulated the system using Re lift P/O LUO converter to improve system efficiency and the results were compared using different converters.

Yang LS. 2018 [27]: introduced a high-step-up DC-DC converter which uses an active switching inductor and a connected inductor to increase voltage conversion ratio and efficiency while maintaining a reasonable duty cycle. Power switches incur less voltage strain. Recycling energy from the leaky inductor can boost efficiency. Using inductors in parallel for charging and in series for discharging on the active switched inductor reduces power switch current stresses.

Tekade AS et. al., 2019 [28]: focused on improving solar panel DC output using the Super-Lift Luo Boost Converter. The Super-Lift Luo Boost converter output voltage grows exponentially. The Super-Lift Luo converter boosts power series voltage transfer gain. After DC/DC conversion, the inverter converts the higher output voltage into AC voltage. MATLAB/Simulink provides a complete Super-lift Luo Boost Converter simulation**.**

Hamid K. Khalil et. al., 2020 [29]: developed and established an MPPT-based positive output super lift POSL LUO converter for photovoltaic (PV) systems Efficiency and limited voltage and current ripple characterize LUO converters. PI controller-based P&O minimizes converter output oscillations and optimizes PV system energy duty cycle. Adjusting PI controller settings requires trial and error.

Zhang X. et. al., 2020 [30] : The suggested converter uses both series and parallel capacitors and a linked inductor for high step-up voltage enhancement.

The coupled inductor's leaking power can help both switches to accomplish zero-voltage shifting, lowering loss of switching and enhancing efficiency. Furthermore, switches and diodes have a lower voltage stress. Low-voltage parts and continuous input current are possible. The converter's operating concept, a steady-state, and parametric design are described.

Ahmed T. Mohammed et. al., [2020] [31]: presented an improved Luo converter with increased output voltage by replacing the inductor with a switched capacitor-inductor cell. His strategy decreases switch stress and boosts growth. The actual and simulated results show 94.1% and 95.4% efficiency.

Hossein Gholizadeh et. al., [2021] [19]: proposed a step-up converter built from cascaded boost and Luo converters. The suggested converter's high efficiency and quadratic voltage gain make it appropriate for energy from renewable sources. the circuit was tested in continuous and discontinuous modes and retrieved and validated the results by testing a 120 W model.

Tohid Rahimi et. al., [2021] [32]: presented converter design parameters such as maintaining input current continuity, positive output voltage, resolving low voltage gain, increasing 10 times lower stresses on semiconductor parts, and achieving 90% efficiency. The test model's design was tested at 100 W output power.

Ream Mohammed Jassim et. al,. [2022] [33]: suggested three alternative PV models for design, implementation, and simulation in MATLAB/Simulink, starting with the boost converter circuit and progressing to the positive output super lift Luo (POSLL) converter circuit. Both circuits were compared to enhance PV system operation and understand how it operates by POSLL

Hussein HAK & H. Motlak [2022] [34]: proposed a modified positive output super-lift Luo converter (POSLC) for significant gain at low duty cycles. Improve effectiveness while reduce switch and diode stress, and minimize inductor current to reduce losses. A hybrid switch unit with four inductors and two capacitors substitutes the fundamental circuit's main inductor. The CCM-DCM boundary condition was developed. Passives supply 8 times D=0.5 the voltage of output and 0.004 ripples. Created and examined the device with MATLAB/Simulink .

Hussein HAK & H. Motlak et. al., [2022] [35] : presented a switched-capacitor cell-based positive output super-lift Luo converter. Charge two capacitors in parallel and discharge them in sequence to enhance output voltage using a capacitive cell. PSIM modeled circuits. Analysis of current, voltage, and gain co-efficient waves corroborated the mathematical calculations. The same programming was used to join the circuit to the maximum power point tracking with a solar cell to maximize energy from the sun utilization using this converter.

Hossein Gholizadeh et. al., [2022] [36]: presented a non-isolated converter with increased voltage gain and a constant input current. His work includes a Luo converter, a quadratic boost converter, and a voltage multiplier cell. At a 50% duty cycle, the voltage gain hits 10 with an efficiency of 91% was built.

Zainab A. Ghafour et. al., [2023] [37]: presented a freestanding photoelectric system using POSLL converter, which might be useful in PV micro converter applications demanding high voltage gain. The device's voltage control results show its benefits. At full load, the converter achieves 95.3% efficiency

Ammar Falah Algamluoli et.al., [2023][38]: introduced a single-cell hybrid switched inductor DC-DC converter to verify renewable energy applications' ultra-high voltage gain. To increase voltage transfer gain, a single inductor cell, diode, and two capacitors are added. This change prevents the input current from reaching zero and causes it to fluctuate at very low duty cycles.

Aseela Sweatha et. al., 2023[39]: introduced a switched-inductor modified LUO converter is introduced for solar-powered water pumps. LUO with switched-inductor type is recommended. This DC-DC converter has a simple design, high voltage gain, low leakage currents, low current ripples, low voltage spikes, low dv/dt stress, and good efficiency. The proposed SI-MLUO converter topology's operating modes and performance are validated using MATLAB/Simulink.

Kumar M. et. al.,2023 [40]: described a three-state switching cell TSSC-based high-gain boost converter. The auxiliary circuit powers switches without electricity or current with the main circuit. The suggested converter has high voltage gain and low switch voltage load. This converter has a voltage multiplier and inductor to enhance voltage. A grid-tied inverter may use this converter's output for green energy..

Vinod Kumar Yadav et. al., 2023[41]: A non-isolated high-voltage gain boost converter benefits from a switched capacitor and decreased switch voltage stress. The proposed construction uses a connected inductor (CI) and switching capacitor (SC) for high voltage gain. CI output low-voltage waves lower output filter capacitor. SC and CI provide a circuit with resonance with zero voltage operation and complete load current switching.

In table (1-1) shows the comparison of DC-DC converter techniques highlights variations in efficiency, gain, losses, and ripple factors. The highest efficiency of 98.7% is achieved by [49], while [26] shows the lowest efficiency at 77%, despite achieving the highest gain of 9. [37] and [34] demonstrate balanced performance with high efficiency (95.3% and 92%) and low ripple (0.022 V and 0.004 V, respectively). Conversely, [29] attains a gain of 4 but suffers from high losses and a significant ripple of 9.54 V, affecting power quality. Most studies employ POSLLC-based converters, with variations integrating MPPT and hybrid switching to enhance efficiency and stability.

In this thesis, the modification of POSLLC based on switched capacitor cell and removing one of its diodes was proposed to enhance the voltage gain and lessen the ripple voltage . The simulation results and the theoretical results showed a matching between them.

Table (1-1) : Performance parameters of POSLC converter

Reference	Efficiency	Gain	Losses	Ripple factor	Used technique
K. Kumar et al.[42]	91.79 %	3	2.343	0.15 V	PI control
S. Jeevananthan et. al. [43]	91.8 %	3	2.316	0.12 V	POSLC
N. Arunkumar et al. [44]	91.8 %	3	2.316	0.12 V	POSLLC
K. R. Kumar et al. [45]	93.6%	4	3.324	0.02 V	POESITBC with ROSMC
Siddharthan N et al. [46]	93 %	3	0.43	24.12 mV	POSLLC.
Malek Guizani et al. [47]	94 %	3	0.6	2.4 V	POSLLC
Nath S et al. [48]	___	6	__	0.47 V	Improved POSLLC
R. Kalaivani et.al [49]	91.8%	3	2.4	0.12 V	FPOSLL
Abid R et al. [26]	77%	9	14	____	POSLLC
Tekade AS et.al [28]	___	3	0	0.022	POSLLC
Ghafour ZA et al. [37]	95.3%	3	7.89	0.2 V	P&O algorithm & MPPT
Hussein Abdul-Khuder Hussein et al. [34]	94 %	8	11.765	0.004 V	Modified hybrid switching
Hamid Khudair Khalil et.al [29]	92%	4	4	9.54 V	P&O algorithm based on PI controller &MPPT
S. Vijai Ananth et al. [49]	98.7 %	3	0.625	1.2 V	ANFIS MPPT
Nazrin Salma S. et al. [50]	93.94%	8	____	____	Modified POSLLC

1.3. Problem Statement

As mention in the introduction and according to many literatures survey, the main issues of DC-DC converters can be summarized as below:

- When the DC- DC converter is extended to get a high transfer gain ratio, the number of components is significantly increased which implies higher sizing and higher cost.
- DC-DC converters consist of the semiconductors like diodes and active switching are suffering from high voltage stress across them due to the weak configuration which causes high heating in these devices and high losses.
- DC-DC converters may exhibit constraints in their ability to convert voltages over a wide range. This might limit their usefulness in voltage conversion applications that demand vast input or output voltage ranges.
- To achieve high efficiency, it is often necessary to employ sophisticated designs and advanced control systems, which can lead to an increase in both design and manufacturing complexity.

Addressing these difficulties necessitates careful consideration of design parameters, component selection, control algorithms, and testing/validation protocols. Innovative solutions, sophisticated materials, and improved manufacturing procedures are constantly being developed to address these issues and increase the performance, dependability, and cost-effectiveness of DC-DC converters.

1.4. Thesis Objective

The objective of this thesis is to :

- Design and simulate of a modified positive output super lift luo converter (POSLLC) based on switched capacitor cell technique at the output and remove one of its diodes, moreover, a multistage switched capacitor cell to enhance the value of voltage gain transfer, minimize the voltage ripple.
- Switched capacitor cells enable the creation of more compressed and lighter converters in comparison to conventional techniques. This is especially beneficial in situations when limitations on space and weight are crucial factors to consider.
- The Modified Positive Output Super-Lift Luo Converter (POSLLC) based on switched capacitor technology offers a solution to the

challenges of achieving high voltage gain while managing design and manufacturing complexity.

1.5. Thesis Contribution

1. Proposed a modified positive output super lift Luo converter with a switched capacitor cell at the output that improves the voltage conversion output voltage gain.
2. A multi switched capacitor cell was incorporated with POSLLC. The converter produces greater voltage levels with less component stress. High voltage conversion ratio applications like renewable energy systems and electronic device power management benefit from this design.

1.6. Thesis Outline

This thesis has five chapters as follows:

Chapter one, involved introduction to converters and its characteristics. The expected outcome of this research is illustrated as well as the objective and contribution of this work .

Chapter 2, involves the theoretical and background information for DC-DC converters and switched capacitor cells .

Chapter 3, involves the design of super lift LUO DC-DC converter and proposed a modified super lift has been investigated. Also, a multi-stage circuit of modified POSLLC based on switched capacitor was presented and compared between them.

Chapter 4, simulation results and the discussion of the results are carried out and demonstrated.

Chapter 5, Shows the conclusions of the thesis and suggestions for future work

CHAPTER TWO

CHAPTER TWO

Theoretical Background on DC-DC Converters

2.1. Introduction

DC-DC converters are electronic circuits that can transform the input voltage to a different level, either higher or lower. It's also called switching technique, due to the effect of the duty cycle on the converter behavior. They are generally called according to their function for instance, converters which are Buck, Boost and Buck-Boost. These converters are used in a large number of power conversion applications such as parts of computers, renewable energy systems and digital systems[10,51] . DC-DC converters can be classified into two main categories: isolated converters and non-isolated converters.

The study focuses on improving prior types of converters, including Luo converters. particular interest is the positive Output Super Lift Luo Converter (POSLC). The converter operates by storing energy in its primary components, namely inductors and capacitors. The inductance stores the magnetic field that generates current, while the capacitance stores the voltage. This energy storage process is achieved by switching the charge pump on and off. The function of a diode is to regulate the flow of current in a circuit, allowing it to be either on or off. This ensures the proper charging and discharging of the circuit [1]. According to this concept, a significant number of DC-DC converter circuits are built to function as either a step-up or step-down voltage, as well as provide either a positive or negative output. Each configuration has its own advantages and drawbacks in terms of efficiency and reliability. The factors considered in [52] include the amount of components, the complexity of the number of switches, the state of shutting and opening each one, and cost savings. Furthermore, the primary function of the converter is to address the pressing requirement of increasing the DC-DC voltage to elevated levels for the purpose of storing and transferring energy. This is necessary as storing energy in batteries necessitates large currents, while transportation demands high voltage [53]. Hence, several contemporary converters exhibit exponential growth to rapidly attain the specified threshold [54].

Increasing the duty cycle is the key to achieving large lift ratios. It must achieve a minimum of 80% of the duration of the prevailing wave. The switch is regarded with great seriousness due to the heightened stress on the switches and the restriction on the lifting voltage. To harness renewable energy sources like sunlight and wind, it is necessary to employ DC/DC circuits for energy tracking and maintaining a stable level. This is because the energy generated from light and wind is variable. Consequently, researchers are focused on developing optimal methods for tracking and utilizing these energy sources[55].

2.2. Operation Modes of DC-DC Converters

The converter design can be based on two modes of operation: Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). These two situations are considered in the design. The inductor amount and load condition required for the converter to operate in (CCM), where the current does not drop to zero, is widely utilized due to its minimal current ripple and higher efficiency. One distinguishing feature of the DCM state is the utilization of a low inductance to get a greater voltage boost, which is desirable for increasing the voltage of the solar cell [72,73]

2.3 DC- DC Converters Classification

It can be classified as bidirectional or unidirectional, current-fed or voltage-fed, and isolated or non-isolated. Step-up converters are categorized into unidirectional and bidirectional designs [56].

Unidirectional boost circuits are appropriate for purposes requiring a one-way energy transfer since they mainly permit energy to pass from the input to the output [57]. Bidirectional boost circuits provide bidirectional power control and storage for energy by controlling the flow of energy in either direction. But they're more complicated and demand more control work [58]. Bidirectional boost circuits perform better than their unidirectional equivalents in various high-power uses. It is because of their benefits in energy recovery, grid integration, lowered component stress, and enhanced management adaptability, in addition to their capacity for reversing the flow of power [59]. Due to these features, bidirectional boost circuits are an appealing option that prioritizes high power quality and system lifespan but requires dynamic and efficient power control techniques [60].

The boost circuits can be assessed by looking at how well they can adjust to changing load currents or stabilize the voltage at the output [61]. The uses involving voltage-sensitive loads can benefit from voltage-fed boost circuits since they concentrate on controlling their output voltages [62]. It exhibits accurate voltage regulation and is frequently employed in applications like voltage regulators. Current-fed boost circuits exhibit improved current regulation outcomes and are more capable of handling fluctuating load currents [63]. They are helpful in situations when load demands fluctuate. Voltage-fed boost circuits are easy to use and reasonably priced. However, they might be unable to handle dynamic loads or bidirectional power transfers [64].

Conversely, current-fed boost circuits perform better in bidirectional processes and are more adaptable to handling load fluctuations [65]. However, they also entail additional parts and require more advanced control techniques. The application objectives are the most critical factor in determining the best option [66].

Without an isolation stage, non-isolated boost circuits are easier to create and cheaper to make. it works effectively when electricity isolation is not a priority [67]. An isolated boost uses electric separation between the source and outputs to improve stability and eliminate ground loops [68]. Due to the isolation elements, they are frequently more expensive, extensive, and ineffective [69]. High-power applications often use isolated boosts due to their reduced electromagnetic interference, improved voltage regulation, flexibility, separation, and voltage stepping [70]. They meet the demanding needs of high-power applications while maintaining control, dependability, and reliability [71]. Figure (2.1) illustrates the fundamental configuration of isolated and non-isolated converters.

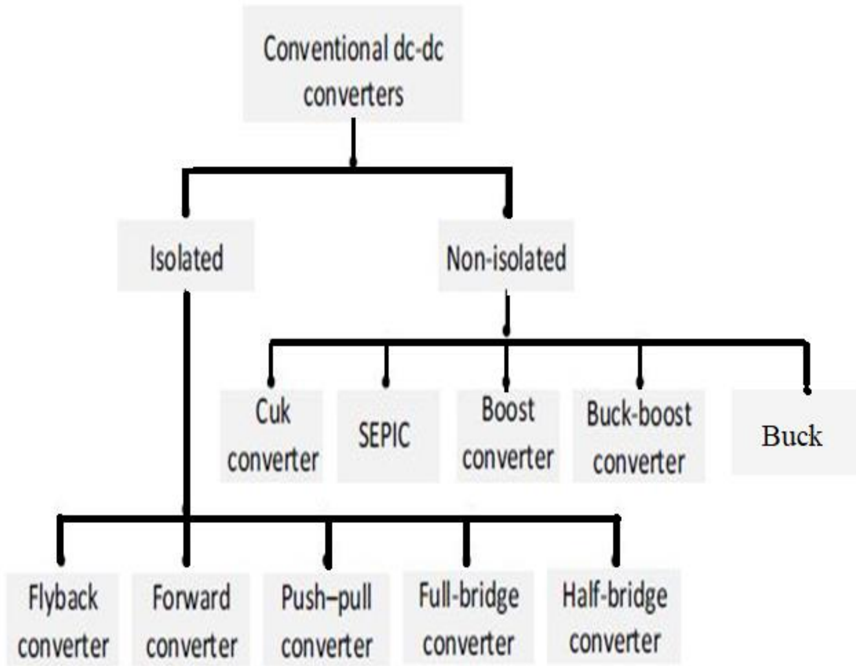


Figure (2.1) Fundamental configuration of isolated and non-isolated converters [10].

Additionally, each of these categories is further classified into two subcategories, namely synchronous and non-synchronous. The synchronous converter incorporates a controllable transistor, whereas the non-synchronous converter utilizes diodes as uncontrolled switches with operational limitations. table (2-1) illustrate the different types of DC-DC converters topologies .

Table (2-1) : Types of DC-DC converters Topologies

Topology	Converters types
Simple	This fundamental category includes the fundamental converters such as Buck ,Boost, and Buck-Boost Topology.
Derived	Positive output Luo converters are among them; they include cuk, double output, negative output, and single ended primary inductance converters (SEPIC).
Topologies with transformers	The converter schemes that use transformer action include the forward converter, push-pull converter, flyback converter, half-bridge converter, bridge converter, and zeta converter.
Voltage Lift	A voltage enhancing technique leads to several topologies, such as the self-lift converter, positive output Luo converter, negative output Luo converter, and double output Luo converters.
Super lift	The voltage gain in the positive / negative output super-lift Luo converter and positive / negative output cascade boost converters has been enhanced through a geometric series.
Ultra lift	The Ultra Lift Luo-converter is a product that boasts exceptional boosting capabilities.

2.3.1. Buck Converter

In recent times, there have been significant advancements in technology, leading to the emergence of various digital devices that aim to enhance our daily lives. However, along with these developments, new challenges have also arisen. One such challenge is the issue of battery depletion and the subsequent need to replace them, which incurs additional costs and obstacles. Consequently, there has been a rise in the demand for battery charging technologies, with a growing trend towards smaller gadgets that are increasingly equipped with batteries [74]. Currently, there is growing interest in creating low-power DC/DC converters, despite the presence of drawbacks such as significant ripple and moderate efficiency. Contrary to expectations, ongoing development also involved efforts to enhance efficiency [75, 76, and 77]. As previously stated, it operates in two cases: Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). It is often built to function in the CCM situation. In this scenario, the buck converter operates when switch is on ,allowing current to flow through the inductor and store energy in the capacitor. When the switch is closed, the energy stored in the inductor and capacitor is transferred to the load, resulting in a mathematical representation of the circuit's behavior as shown in figure (2.2). The task involves reducing the voltage in a step-down manner [78,79,80]. the output voltage equation for Buck converter is : $Vo = K\ Vs$

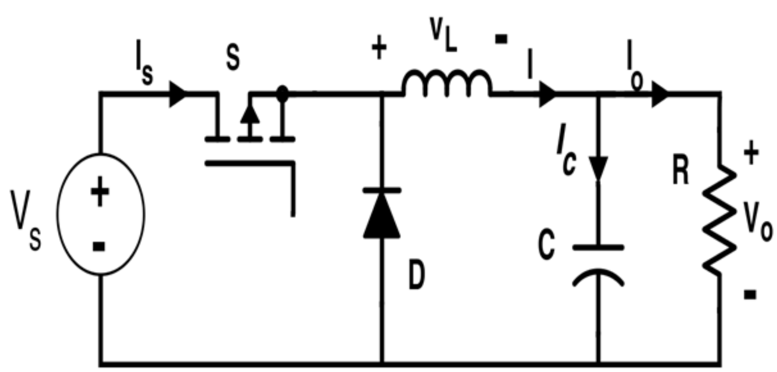


Figure (2.2). Buck converter circuit [87].

2.3.2. Boost Converter

When utilizing a converter, it is typically necessary to increase the voltages beyond the previous levels for various purposes, such as meeting the demand for a higher voltage load from the source or facilitating energy transmission, as seen in renewable energy systems like wind energy. Photovoltaic panels must maintain a consistent voltage despite fluctuations in the load, as the voltage is always impacted. This is accomplished by a control circuit. In this field, the boost circuit seen in figure 2.3 is the initial component that has been employed [78]. The pace at which the voltage is increased during lifting is influenced by the speed of the switch (frequency and duty cycle). Additionally, the efficiency is reduced due to increased voltage caused by losses in the diode [81]. The device typically functions in (CCM) and identifies the switch-ON condition as the current channel from the source to the inductor. The magnetic field is transformed into an electric current when the switch is turned off, causing the inductor to be in an OFF state. The gain equation for boost converter is $G=\frac{1}{1-K}$.

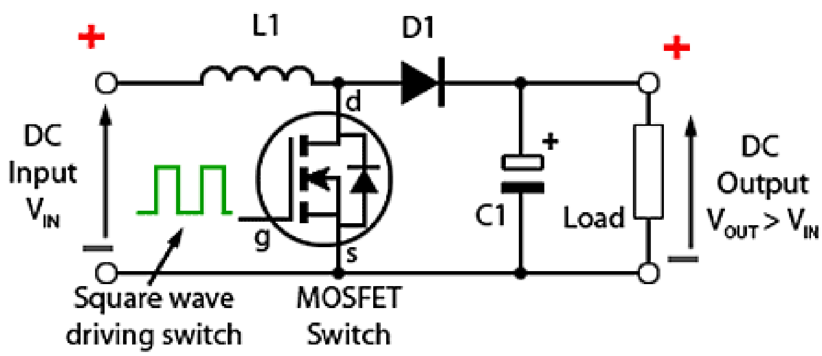


Figure (2.3). Boost-converter [86]

2.3.3. Buck-Boost Converter

The buck-boost converter is a type of DC/DC converter. It operates in the third quadrant. The buck-boost refers to the integration of a buck step-down converter with a boost step-up converter. The output of the switches is depending upon their switch-duty [83,84]. The operation of a buck-boost converter is comparable to earlier systems in terms of the inductor and switching mechanism, but it distinguishes itself through its unique structure. Indeed, it possesses the advantages of integrating the preceding strategies in terms of elevation and descent. The gain equation describes the functioning of the system, and the necessity for regulation of renewable energy sources arises due to fluctuations in their availability, making this sort of energy appealing. Other converters that can be used for buck-boost applications include CUK, SEPIC, and ZETA [1, 52]. The basic buck-boost circuit, seen in figure 2.4, comprises a power switch, an inductance, a diode, a capacitance, and a load [78,85]. When the buck-boost circuit's switch is in the ON state, the inductor is charged and the diode is in reverse bias, acting as an open circuit. This isolates the load from the source, allowing only the current to flow through the inductor. In the second scenario of buck-boost circuit operation, when the switch is turned off, the inductor acts as a source of power, supplying it to the capacitor. The diode operates in a forward biased manner to allow the current to pass through the circuit. In the second cycle of the switch (2nd ON), the inductor is reconnected to the source, while the diode is biased in the opposite direction to isolate the rest of the circuit. The capacitor acts as the power source to discharge into the load. The electric current is directed towards the load. It should be noted that the output voltage is generated when the circuit changes polarity, which is caused by the polarity of the capacitor. In the second OFF state, the inductor acts as a source of energy to charge the capacitor, and the diode completes the current path when it is forward-biased [84]. The specifics of the buck-boost converter and its mathematical model, including all relevant equations, can be found in reference [85].the gain equation for buck boost converter is : G= $\frac{K}{1-K}$

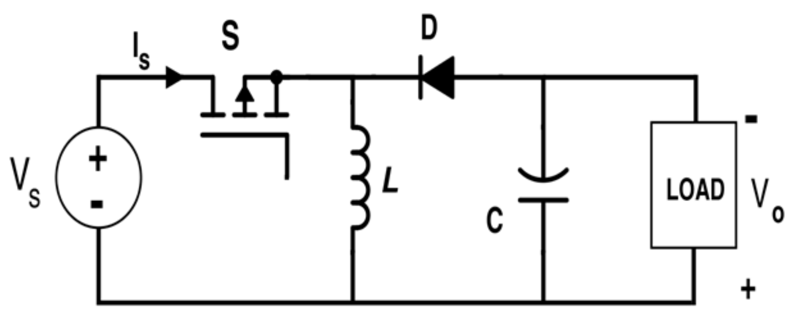


Figure (2.4).The buck boost converter's equivalent circuit [87]

2.4 LUO Converter

The LUO converter is a type of DC/DC converter that is derived from Buck Boost converters. It is known for its high voltage transfer gain and minimal ripple in voltage and current. The LUO converter exhibits superior efficiency in comparison to non-isolated DC-DC converters [88]. The converter's output voltage exhibits minimal ripple with a value that is below 2% [89]. The output of the LUO converter can either exceed or be less than the input voltage. The LUO converter utilizes techniques such as Voltage Lift

(VL) and Super Lift (SL) to effectively increase the voltage [90]. In the design of a high voltage gain converter, (VL) techniques are employed to raise the output voltage in an arithmetic progression, while (SL) techniques are used to increase the output voltage in a geometric progression. According to reference [10], the (SL) technique is more effective than the (VL) technique.

2.4.1 Voltage Lift Technique

The technique of Voltage Lift(VL) is an efficient technology for rising the output voltage used in the design of electronic circuits to get rid of parasitic elements and increase the Voltage Transfer Gain (VTG) of significantly. (VL) Technology is used in DC-DC converters that operate for higher voltage output. The principle of the technology of (VL) is the introduction of more elements of the capacitors and inductors to store energy and this leads to improve the performance of converters. To improve circuit properties voltage lift technique are used and applied to DC converters successfully. Three LUO converters developed using (VL) technique. These converters work very efficiently with a simple structure and different from such converters commonly used in computer peripherals and have many benefits, including high output voltage and low ripple, industrial applications and high voltage projects[91]. the work of these converters is positive to positive with high voltage and high efficiency with simple structure. Three converters from the LUO series developed from prototype models using(VL) technology are self-lift, re-lift and multiple-lift [92]. The figure shows the classification of DC-DC Luo converter.

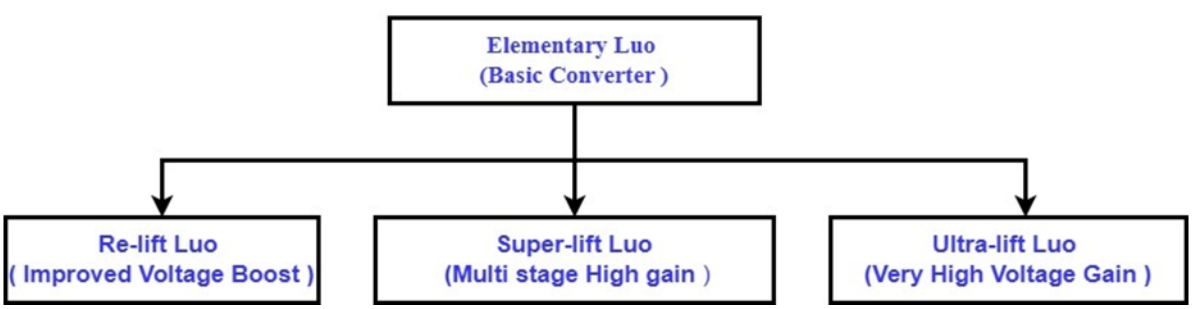


Figure (2.5) .The classification of DC-DC Luo converter**.**

The table below shows a comparison between the types of DC-DC Luo converter.

Table (2-2): comparison for the types of DC-DC Luo converter.

Classification	Number of Stages	Voltage Gain Ratio	Efficiency	Applications
Elementary Luo	Single stage	Low	Moderate	Low-power Electronics
Re-lift Luo	Two stages	Medium	Good	Medium power systems
Super-lift Luo	Multiple stages	High	Excellent	Renewable energy systems
Ultra-lift Luo	Highly multiple stages	Very high	very high	High-voltage applications and renewable energy

2.4.1.1 Positive Output LUO-Converter

The circuit depicted in Figure (2.6) is a DC/DC converter that can both step down and step up the voltage. Positive output LUO-converters employ a voltage boosting technology to convert a positive voltage into higher positive voltages. The POLC (Power Optimized Lifting Converter) is obtained by modifying the fundamental circuit. The modified converters include self-lifting, re-lifting, and multi-lifting circuits [6].

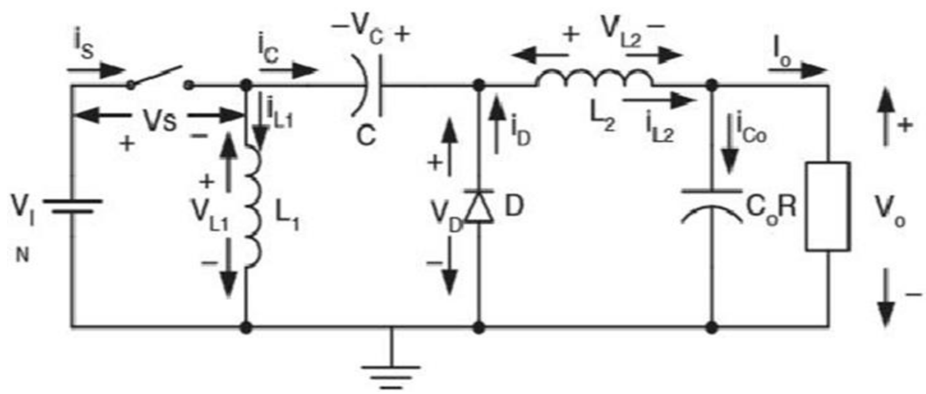


Figure (2.6). POLC Circuit [6].

2.4.1.2 Elementary Circuit Description of Positive Output LUO-Converter

The capacitor (C) in the circuit depicted in Figure 2.7 functions as an energy storage and transfer device between the input source and the load, facilitated by inductor L_1 [6].

The LUO positive output elementary circuit converter has two operating modes, which vary depending on the shift circumstance. During the on state, the current traveling through is denoted as I_S while the circuit is closed, and it is equal to the sum of I_{L1} and I_{L2}, represented as $I_S = I_{L1} + I_{L2}$. The primary purpose of both inductors, L_1 and L_2, is energy absorption. L_1 absorbs energy from the source, whereas L_2 absorbs energy from both the capacitor and the source. In this scenario, the currents I_{L1} and I_{L2} are seeing an increase. The circuit is depicted in Figure 2.7 .

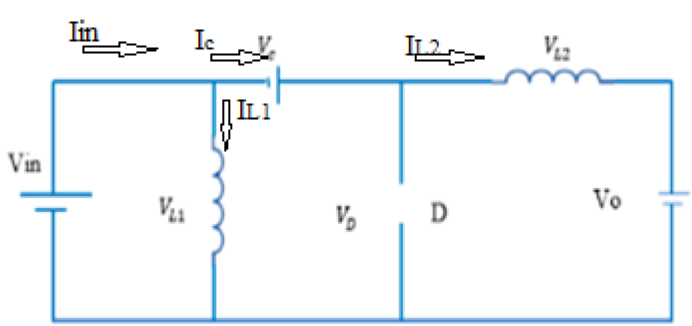


Fig.(2.7). The circuit when the switch is on [119].

During switch off state, When the switch is opened, the source current (i_s) becomes zero and the energy stored in L_1 is transferred to the capacitor (C). At the same time, the current (i_{L2}) flows via the circuit (C_O - R) and the freewheeling diode D to maintain a constant value. The present (iL1) passes via the free-wheeling diode (D) in order to charge capacitor (C). The magnitudes of the currents i_{L1} and i_{L2} drop. The circuit is depicted in Figure 2.8.

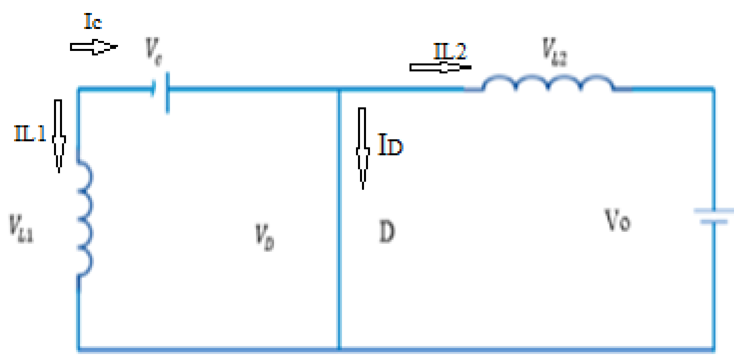


Figure.(2.8).The circuit when the switch is off [119].

2.4.2 Super Lift Technique

The super lift (SL) technique is a commonly employed approach for increasing voltage [92].The super lift technique (SL) incrementally raises the output voltage along the engineering progression [93]. The voltage transfer gain in the power series has been enhanced with the implementation of the super lift technology [94]. The voltage boost method is extensively utilized in electronic circuits, with the (SL) technique being regarded as superior to the (VL) technique for power transfer in all converters [95]. Typical circuits are categorized into four series: Positive Output Super Lift LUO (POSLL) converters, Negative Output Super Lift LUO (NOSLL) converters, positive output cascade boosters, and negative output cascade booster converters. Super-lift converters utilize engineering advancements to achieve high gains, whereas voltage lift converters gradually improve gain in stages. The converters are currently focused on enhancing the power series [91,96] to get higher gains.

2.4.2.1 Negative Output Super-Lift LUO Converter

The super lift negative output LUO converter incrementally increases the output voltage at each stage of the geometric process, hence improving the voltage transfer gain according to the energy law. The NOSLL Converter has good efficiency and a low level of ripple [97] . The circuit diagram of the (NOSLL) converter is shown in Figure 2.9. The negative output converter has one inductor, two capacitors, and two diodes, together with a load [98].

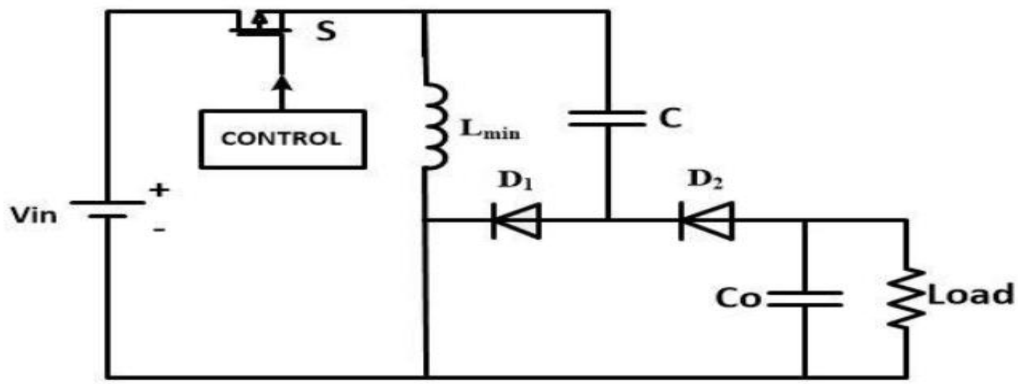


Figure (2.9). NOSLC Circuit [98].

2.4.2.2 Elementary Circuit Description of Negative Output Super-Lift LUO Converter

Figure (2.9) depicts the primary circuit of the negative output super lift LUO converter, as well as its comparable circuits during switch-on and switch-off. The voltage across capacitor C is increased to the value of V_{in}. The current passing through inductor L_1 rises with a gradient of V_{in}/L_1 during the switch-on period KT and declines with a gradient of $-(V_o - V_{in})/L_1$ during the switch-off period (1 - K)T [97].

The negative output super-Lift Converter elementary circuit features two operating modes that rely on the switch state.

In active state, when the switch is on , the current flows through the L_1 inductor and the capacitor. The C_1 capacitor is being charged to the V_{IN} input voltage. The diagram of the circuit is depicted in Figure 2.10.

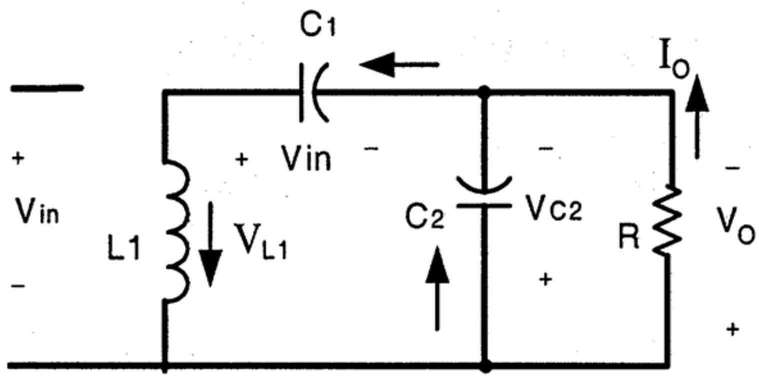


Figure (2.10) .Switch-ON mode[6].

During this time interval, the electric current flowing through the inductor L_1 will experience an increase that is proportional to the rate of change of the input voltage Vin divided by the inductance L_1.

Hence, the change in current in L_1 during the ON period of KT will be

$$\Delta iL_{1\,ON} = \frac{Vin}{L_1} KT \tag{2.1}$$

In off state when the switch is turned off, the load discharges the capacitor and inductor L_1,C_2. The electrical current in the inductor will go down because it provides the load and C1.The circuit can be seen in Figure 2.11[99].

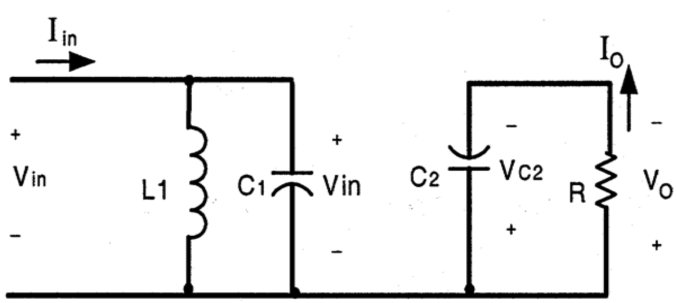


Figure (2.11). Switch-OFF mode [6].

To find the voltage in the L_1 inductor, look at Figure above. It says that the voltage is $-(V_O-V_{in})$ or $(V_{in}-V_O)$.

Because of this, As a result, the current going through the inductor drops by

– $(V_O – V_{in})/L_1$.

This is because its known that the time it takes for the switch to turn off is

(1 -K)T.

So there is a change in current, It is written as

$$\Delta iL_{1OFF} = \frac{-(Vo-Vin)}{L_1}(1-K)T \quad (2.2)$$

If $\Delta i_{L1}ON$ is less than Δi_{L1OFF},

This means that $\frac{Vin}{L1}KT = \frac{(-(Vo-Vin))}{L1}\ (1-K).T$

By making it easier,

$$V_{in}\frac{1}{1-K} \quad (2.3) V_O =$$

Where V_o is the output voltage .

2.4.2.3 Positive Output Super-Lift LUO Converter (POSLLC)

The POSLLC exhibits superior performance in terms of exceptional voltage enhancement, high voltage amplification, high power concentration, and little output voltage fluctuation. The POSLLC circuit is utilized for increasing the DC voltage, while certain circuits can also be employed for decreasing the voltage. These circuits exhibit similar performance to a buck boost converter [100]. The super-lift LUO converter amplifies the output voltage by boosting its positive polarity, hence enhancing the transmission voltage gain [29]. The POSLLC converter is partitioned into sub, major, and additional components. The primary circuit comprises a switch, inductor, and two capacitors, with two diodes linked to the load. The components of the POSLLC are determined through the utilization of specific formula for each individual part [101]. The primary series consists of three circuits in the high positive output LUO converter, which are referred to as the Elementary circuit, Re-lift circuit, and Triple-lift circuit. The elementary circuit is depicted in Figure 2.12.

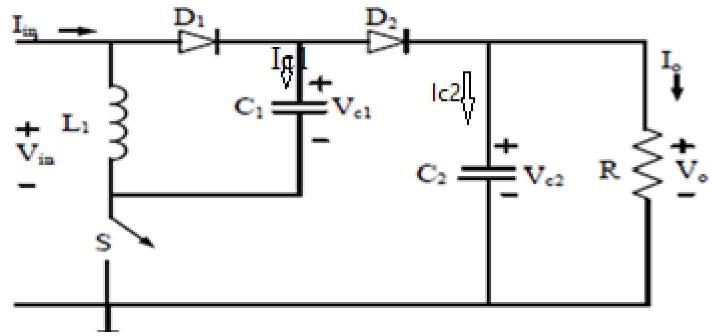


Figure (2.12). POSLC Circuit [29]

2.4.2.4 Elementary Circuit Description of Positive Output Super Lift LUO Converter

As shown in figure (2.12) ,the elementary circuit with a positive output. When the switch is closed, the capacitor is charged with the input voltage value. The current passes through the L_1 inductor and rises during the switch-on period (KT) with the input voltage V_{in}. During the switch-off state , the current flowing through the inductor, denoted as iL_1, falls in proportion to the negative voltage $-(V_O-2V_{in})$. This occurs for a duration of (1-K)T [102].The POSLLC is comprised of a switch S, an inductor L, two diodes (D1 and D2), two capacitors (C_1 and C_2), and a resistive load (R). The fundamental circuit of POSLLC operates in two modes, which are determined by the switch state . During on state, when the switch is closed, the equivalent circuit of positive output super lift LUO converter is shown in Figure (2.13). The diode D_1 is forward biased and the diode D_2 is reverse biased in this mode input is connected to the inductor L_1 and capacitor C_1 .The capacitor C_1 is charged to V_{in}. The current through the inductor L increases with the input voltage Vin. The input current (I_{in}) during mode 1 (on state) is equal to ($I_{L1} + I_{C1}$).

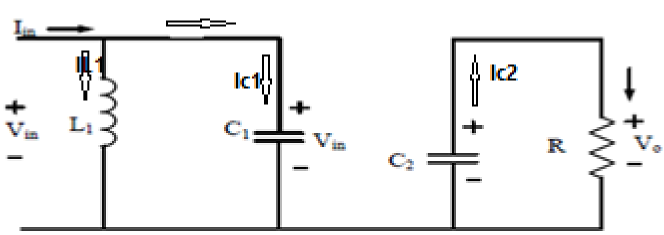


Figure (2.13). Switch-ON mode [29]

According to Kirchhoff's law when the switch is ON [92] ,

$$V_{in} = V_{L1} = V_{C1} \tag{2.4}$$

The inductor voltage is: V_L

$$V_L = L\, \Delta I/\Delta t \quad ` \tag{2.5}$$

By Kirchhoff's current law

$$I_{in} = I_{L1} + I_{C1} \tag{2.6}$$

Where I_{in} is the input current , I_{L1} is the inductor current and I_{C1} is the capacitor C_1 current .

$$I_O = I_{C2} \tag{2.7}$$

Where I_o is the output current and I_{C2} is the capacitor C_2 current .

the ripple current of inductor Δi_L is :

$$\Delta iL = \frac{V_{in}}{L}\, KT = \frac{Vo-2Vin}{L} KT \tag{2.8}$$

$$V_o = \frac{2-K}{1-K} V_{in}\ ,\ I_o = \frac{2-K}{1-K}\, I_{in} \tag{2.9}$$

V_o is the output voltage and I_o is the output current .

Now, the average input current is :

$$i_{in} = i_{L1} + i_{C1} \tag{2.10}$$

$$i_{in\text{-}on} = i_{L1\text{-}on} + i_{C1\text{-}on} \tag{2.11}$$

$$i_{in\text{-}off} = i_{L1\text{-}off} = i_{C\text{-}1off} \tag{2.12}$$

$$i_{in\text{-}on} = I_{L1} + \left(\frac{1-K}{K}\right) IL1 = (2 - K)\, I_{L1} \tag{2.13}$$

$i_{C1\text{-}on} = \left(\frac{1-K}{K}\right) IL1$, The average current is calculated using this equation is as follows:

$$I_{in} = K i_{in\text{-}on} + (1\text{-}K)\, i_{in\text{-}off} = I_{L1} + (1 - K)\, I_{L1} \tag{2.14}$$

Thus , the variation ratio of current i_{L1} through inductor L_1:

$$\xi = \frac{\Delta iL1/2}{IL1} = \frac{K\,(2-K)\,T\;Vin}{2\,L1\,Iin} = \frac{K\,(1-K)^2 R}{2\,(2-K) f L1} \tag{2.15}$$

Output voltage Vo's ripple voltage is :

$$\Delta_{Vo} = \frac{\Delta Q}{C2} = \frac{Io\,(1-K)}{C2} = \frac{(1-K)\,Vo}{f\,C2\,R} \tag{2.16}$$

Therefore, the variation rate of output voltage as :

$$\varepsilon = \frac{Vo/2}{Vo} = \frac{1-k}{2\,R\,f\,C2} \tag{2.17}$$

The output capacitance Co may be computed using the equation below [33]:

$$\Delta_{Vo} = \frac{(1-K)}{fCo}\frac{Vo}{R} \tag{2.18}$$

The transfer gain (G) formula is given by the equation:

$$G = \frac{Vo}{Vin} = \frac{(2-K)}{(1-K)} \tag{2.19}$$

$$V_O = \frac{(2-K)}{(1-K)}\;Vin \tag{2.20}$$

When the switch is turned off, the circuit that represents the positive output super lift LUO converter is shown in Figure (2.14). Diode D1 is experiencing a reverse bias, whereas diode D2 is experiencing a forward bias. During the switching-off time, capacitor C1 and inductor L1 are connected in series with capacitor C2. The current I_{L1} flowing through the inductor is equal to the current I_{C1} flowing through the capacitor. When the switch is turned off, the inductor current falls [103,104].

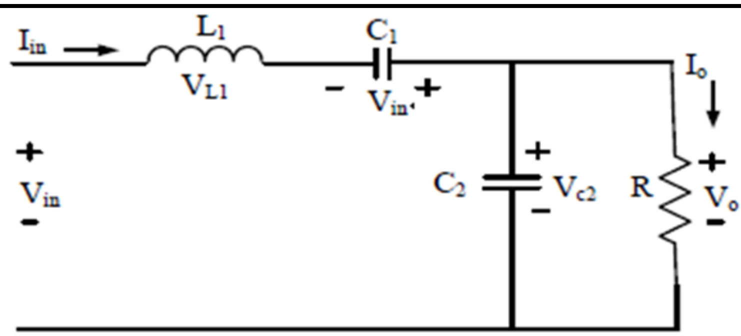


Figure (2.14) .Switch-OFF mode [29].

By Kirchhoff's voltage law in a circuit (OFF mode)

$$V_{in} - V_{L1} + V_{C1} = V_{C2} \tag{2.21}$$

By Kirchhoff's current law,

$$I_{in} = I_{L1} = I_{C1} \tag{2.22}$$

The passing current in the capacitor C1 is: I_{C1}

$$I_{C1} = I_{C2} + I_O \tag{2.23}$$

Now assuming that capacitor C_1 charges to the input voltage,

$$V_{C1} = V_{in} \tag{2.24}$$

Substituting (2.24) in (2.21), to obtain,

$$V_{in} - V_{L1} + V_{in} = V_{C2}$$

$$-V_{L1} + 2V_{in} = V_{C2} \tag{2.25}$$

In OFF mode, the inductor voltage is

$$V_{L1} = -L1\frac{\Delta I}{T_{OFF}} \tag{2.26}$$

Where T_{OFF} is the time taken for OFF mode,

$T_{ON} = KT, T_{OFF} = (1 - K)T$ and simplifying we get,

$$V_{C2} = 2V_{in} + \frac{K}{1-K}V_{in} \tag{2.27}$$

But according to ON mode, $V_o = V_{C_2}$

$$V_o = 2V_{in} + \frac{K}{1-K}V_{in} \tag{2.28}$$

The ratio of the time taken for mode 1 (during ON time) to mode 2 (during OFF time) is now being computed.

$$\frac{T_{ON}}{T_{OFF}} = \frac{V_O - 2V_{in}}{V_{in}} \tag{2.29}$$

The switching period in the first and second mode is, T

$$T = T_{ON} + T_{OFF}$$

$$I_{inOFF} = I_{L1} = I_{C1} \tag{2.30}$$

$$I_{inON} = I_{L1} + I_{C1} \tag{2.31}$$

$$\frac{V_{in}}{I_{in}} = \left(\frac{1-K}{2-K}\right)^2 R \tag{2.32}$$

The capacitor ripple voltage on the output side is given as,

$$\Delta V_{C_2} = \frac{I_o}{fC_2}\left[\frac{V_o - 2V_{in}}{V_o - V_{in}}\right] \tag{2.33}$$

$$V_o = V_{C_2}$$

$$\Delta V_o = \frac{(1-K)}{fC_2R} \times V_o \tag{2.33}$$

The voltage gain G

$$G = \frac{V_o}{V_{in}} = \frac{2-K}{1-K} \tag{2.34}$$

according to the table (2.2) in comparison of (POSLC) with other traditional converter, can see that the (POSLC) is produce large output voltage gain than other converter that used one active switch only. The CUK converter is the same of Luo in gain equation but CUK is negative and used less number of elements.

Table (2.3): Comparison between the positive output super- lift Luo converter and some basic boost converters .

Attributes	Conventional boost converter					
	Buck	Boost	Buck-boost	Cuk	Positive output luo	POSLC
Voltage gain expression	K	$\frac{1}{1-K}$	$\frac{K}{1-K}$	$\frac{-K}{1-K}$	$\frac{K}{1-K}$	$\frac{2-K}{1-K}$
Gain at D=0.5	0.5	2	1	1	2	3
No. switches	1	1	1	1	1	1
No. of components	3	3	3	5	6	5
No. of diodes	1	1	1	1	2	2
High/low side gate driver	High	Low	High	Low	Low	High
Common ground	Yes	Yes	Yes	Yes	Yes	Yes

2.5. Component Losses of DC/DC Converter

The voltage across both terminals of the switch is generated by the rate at which the switch is toggled between the ON and OFF positions. When the switch is in the ON position, the voltage does not decrease to zero and the current rapidly increases simultaneously, leading to losses due to the fact that the voltage and current are changing at their maximum ranges. This will lead to a decrease in power. The primary source of losses stems from the substantial quantity of components. During rapid switching operations, the presence of many diodes results in certain losses, while the presence of multiple switches also leads to losses. Losses can be minimized by decreasing the quantity of components and selecting the suitable diode. In switching scenarios, the frequency can be decreased and MOSFETs can be employed as a substitute for conventional transistors.

To minimize losses during the switching process, one can utilize either the resonance process or the resonant frequency [54]. The use of a transformer and passive components in isolated converters worsens the loss. One way to reduce converter losses is by using a transformer to isolate the load current from the source current, which also isolates the converter from the source voltage. In order to minimize losses, it is advisable to operate the converter in

Continuous Conduction Mode (CCM), since this also reduces the frequency of the switch's operational noise [105].

The ripple in the converter consists of two types: voltage ripple, which is produced by the boost capacitor C1, and current ripple, which is produced by the inductor L. These two parts are the major components of the converter. In order to minimize the presence of fluctuations, it is necessary to implement a filter at the output of the converter. However, in the suggested converter, we have included an inductor at the output before the load, which effectively reduces the ripple [106].

2.6 Cell technique (Voltage Multi Cell)

There are several methods to increase voltages, but, each method possesses its own set of restrictions, benefits, and drawbacks. One factor is the control circuit of the switch, which increases the duty cycle. The main Lifting converters need to work within a specific range of duty cycle values, from 0.1 to 0.9. Increasing the duty cycle will result in greater voltage. This also applies to buck converters [107]. However, there are constraints. An increase in the duty cycle causes the switch to operate more frequently, resulting in higher losses due to temperature and reduced efficiency. Furthermore, the voltage can be improved by increasing the frequency. However, it is important to note that operating the switch at exceedingly high frequencies might impose constraints and give rise to additional losses due to the inability to fully deactivate the switch while in the OFF state.

Another method to increase the voltages is by utilizing multiple stages (cascade-connect) of the same converter. However, there are limitations to how much the voltage can be raised, as it will decrease if the number of stages exceeds a certain threshold. Additionally, the cost of the circuit increases due to the additional components required for this approach.

Another method for increasing voltages involves the addition of inductance or capacitance at specific locations. The capacitance technique, known as the switched capacitor (SC) method, primarily relies on a charge pump (CP) circuit commonly used in converters to boost voltages. The capacitive power switch is solely responsible for the enhancement of voltage levels in the (CP) circuit. Many strategies for circuit design, including as CP (complementary push-pull) and single-ended topologies, are commonly employed due to their structural simplicity and ability to integrate lift voltage.

In Figure (2.15), there are two switches that alternate between being turned on and off. When switch A is turned on, capacitor C_1 charges until it reaches the same voltage level as the input. When switch B starts to turn on, the stored electricity in C_1 is transferred to capacitor C_2. The switches alternate in this manner. This approach is referred to as transferring energy from one capacitor to another, and after several cycles, the output voltage achieves the desired voltage level. Currently, it no longer produces large lifting voltages, but it is an improvement over previous versions since it exhibits lifting voltages that follow a geometric sequence and have greater values. The following study focuses on the usage of the cell, which is the most superior way among the previously described options.

This method offers several benefits for increasing voltages and is regarded as a groundbreaking advancement in the field of DC/DC converters. Notable properties of this converter include exceptionally high lifting values, compact size, and rapid voltage acquisition due to a minimal transition duration compared to other methods that employ geometric sequences. Additionally, there is a minimal number of components [108]. Hence, analyze the many categories and configurations of the cell, together with the techniques employed to link it in the converter and its functioning, as depicted in figure 2.16. These include: (A) switching capacitor cell, (B) switching inductor cell, and (C) hybrid switching inductor-capacitor cell, which will be discussed subsequently.

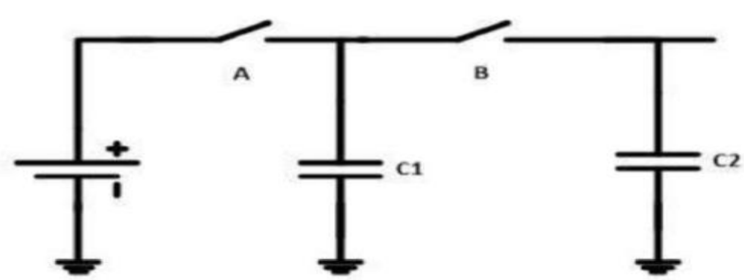


Fig (2.15): Basic charge pump[1]

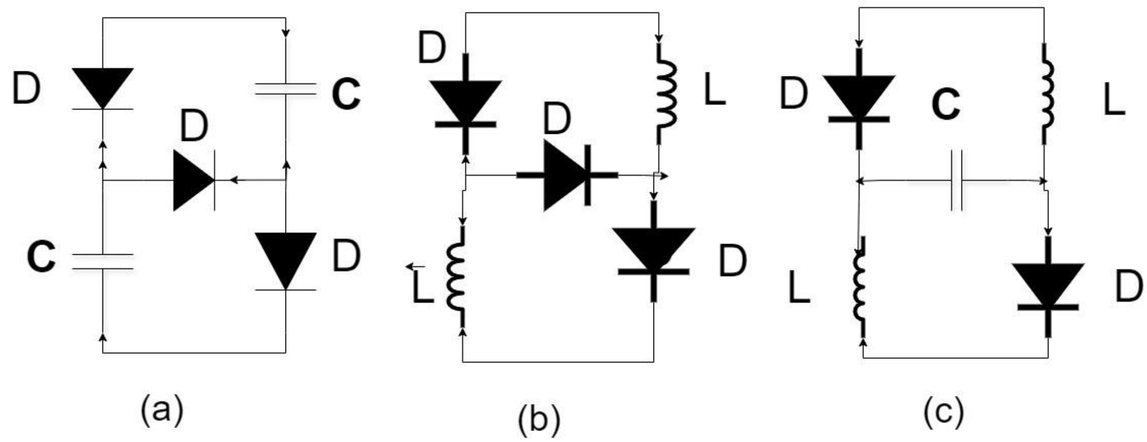


Figure (2.16). Voltage multiplier cell a) switching capacitor cell b) switching Inductor cell c) hybrid switching inductor-capacitor cell [1]

Many cell types boost voltage. They can regulate it with switches and another in the shape of a star and delta . The cell-connected technology with diodes, capacitors, and inductors to increase voltage . In dc/dc converters, it can replace the inductor with a cell.

Modifying a Positive Output Super Lift Luo Converter (POSLC) with switched capacitor cells has many benefits. First, these cells amplify voltage, allowing the converter to output higher voltages. It's useful in circumstances that require higher voltage. Effective energy transmission across capacitors enhances converter efficiency, minimizing energy waste and power transfer. Switched capacitor cells reduce output voltage ripple, ensuring a more stable output voltage for sensitive electronics. Their inclusion allows the fabrication of tiny, lightweight converters that can overcome space and weight constraints in various applications [109]. The used switched capacitor cell shown in the figure below.

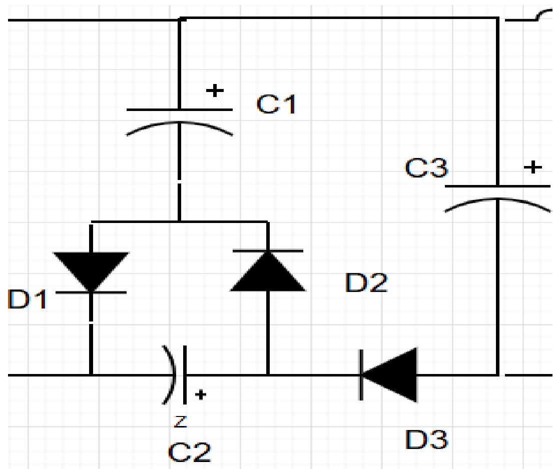


Figure (2.17) .The used switched capacitor cell

Switched capacitor cells provide a wide range of input and output voltage combinations due to their voltage conversion ratios. The increased POSLC's flexibility increases its application versatility. Included cells improve converter performance, including transient responsiveness, voltage control, and load regulation. Adding switched capacitor cells to the enhanced POSLC makes it flexible and efficient for many power conversion applications.

CHAPTER THREE

Chapter three

The proposed modified Positive Super Lift Luo DC-DC Converter Based on Multi Switched capacitor cell

3.1 Introduction

At the beginning of this chapter, the work focuses on the design and mathematical analysis of the modified Positive Output Super-Lift Luo Converter (POSLLC) based on the Multi-Switched Capacitor Cell (MSCC) technique, operating in Continuous Conduction Mode (CCM). Additionally, the equations governing the modeling of the POSLLC circuit with MSCC are explained. Furthermore, this chapter presents an analysis of the control unit and the rationale for its implementation. Figure 3.1 shows the layout configuration of the proposed system.

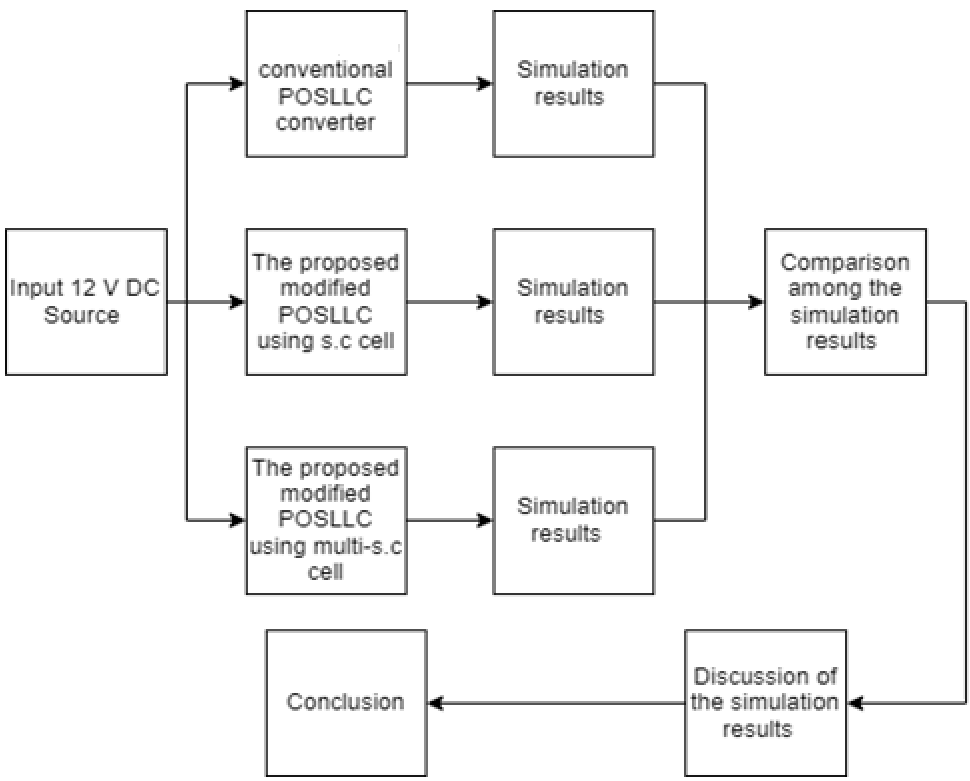


Figure (3.1). the layout of the proposed system

3.2 The Conventional (POSLC) Circuit

The conventional circuit of (POSLC) is clarified theoretically in chapter two (section 2.4.2.4). The simulated elementary POSLC circuit is offered in this chapter. Some features are lift voltage and fast response control to load conditions with a source drop in the same time. Figure (3.2) shows the simulated circuit of the conventional POSLLC.

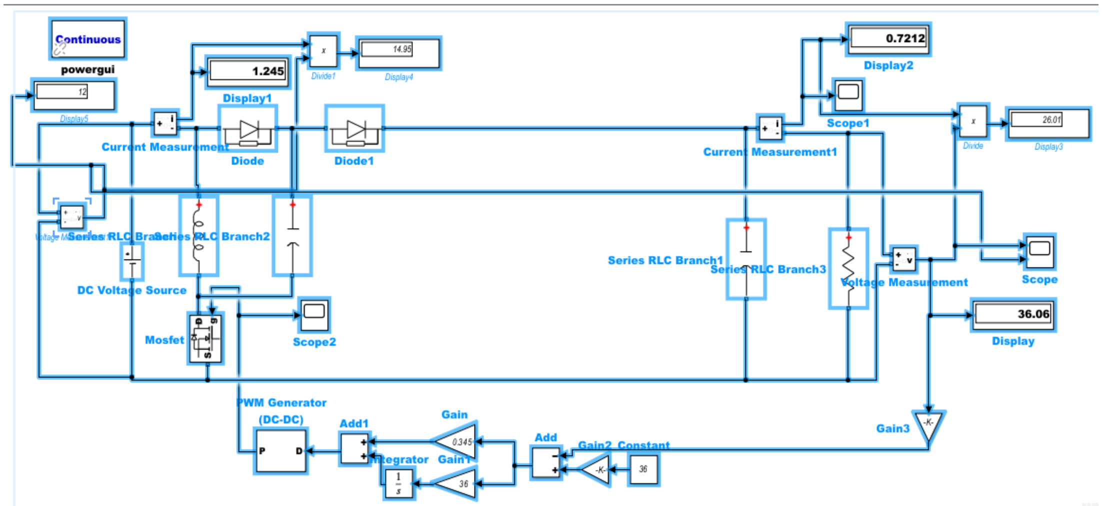


Figure (3.2) . the simulated circuit of conventional POSLLC

3.2.1. The Parameters of Elementary (POSLC) Circuit

From the equations presented in chapter two , we can design the values of the inductor, boost capacitor (C_1) and output capacitor (C_o) in figure (2.13) under the following assumptions.

Design parameters:

Duty cycle (K) = 0.5

Input voltage (Vin) =12 v

Switching frequency (F_s) =100 kHz

From equation (2.20) yields 36V output voltage.

Since it is the variation ripple (ζ_L) of inductor current unknown, we can choose from (0.2 - 0.4).

We can choose variation ripple $\zeta L = 0.4$. From equations (2.8) can obtain the numerical value of the inductor L_1.

Its L_1=100μH .

A capacitor is used to reduce the voltage ripples, so you should choose a high value to reduce the ripples output Luo converter. The minimum ripple value in voltage must be chosen for the design of the capacitor. The capacitor value can

be calculated from the equation in Chapter 2 of the Luo converter. Therefore, the output ripple voltage from luo converter is approximately 0.06V.
the numerical value of the capacitor can be obtain from equation (2.18) =30µF. the table below shows the parameters of conventional circuit.

Table 3.1:The parameters of Conventional Circuit

Parameter's name	Symbol	Value
Input voltage	Vin	12 V
Output voltage	Vo	36 V
Inductor	L_1	100µH
Capacitors	C_1,C_2	30µF
switching frequency	F_s	100KHz
Load resistance	R	100
Duty cycle	D	0.5

3.3 The Proposed Modified LUO Converter

Figure (3.3) shows the proposed model being considered. As explained in the introduction, this suggested converter's main advantage is that it can work with low-voltage supplies like batteries, fuel cells, and photovoltaic systems. The converter's primary goal is first to increase these supplies' voltage output, followed by improvements to the converter itself. The switched-capacitor (SC) cell, composed of capacitors C_2, C_3, and C_4 and diodes D_2, D_3, and D_4, enhances the voltage. The SC structure demonstrates that the output voltage gradually distributes into the power switch and the capacitors, reducing the voltage impact on the electronic components.

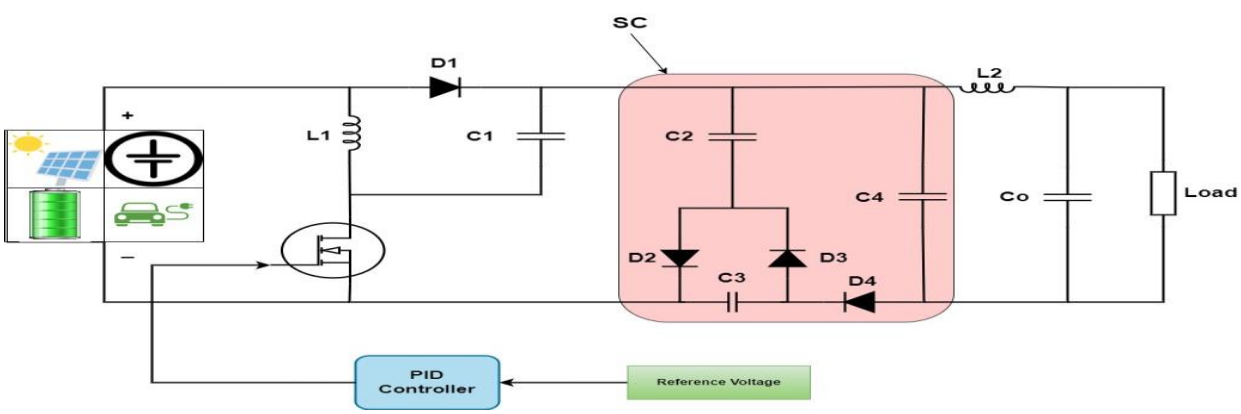


Figure (3.3). The Proposed SC Luo converter.

3.4 Operation Analysis

Figures (3.4) and (3.5) show the status of the semiconductor switch and the charging and discharging processes for capacitors and inductors. Figure (3.4) illustrates the switch's conduction condition, which occurs when the switch receives a positive pulse from the PWM switching signal. During operation, the switch S_1 and input voltage source Vin are encircled by loops formed by the inductor L_1 charging from the source. Capacitor C_1 is charged concurrently by the input source via switches S_1 and Diodes D_1. Regarding the SC cell, in this operating mode, capacitor C_3 is charged through diode D_3 by discharging capacitor C_2, and diode D_2 is reverse-biased. It is important to remember that capacitor C_4 provides a steady output voltage for the load in this setup because the connectivity across the input and output ends is removed. Thus, it could be summarized as follows for this particular operation mode:

$$V_{L1} = L_1 \cdot \frac{di_{L1}}{dt} = V_{in} \quad (3.1)$$

$$V_{C1} = V_{in} \quad (3.2)$$

$$V_{\text{in}} = V_{C2} - V_{C3} \quad (3.3)$$

$$V_{C4} = V_{L2} + V_O \quad (3.4)$$

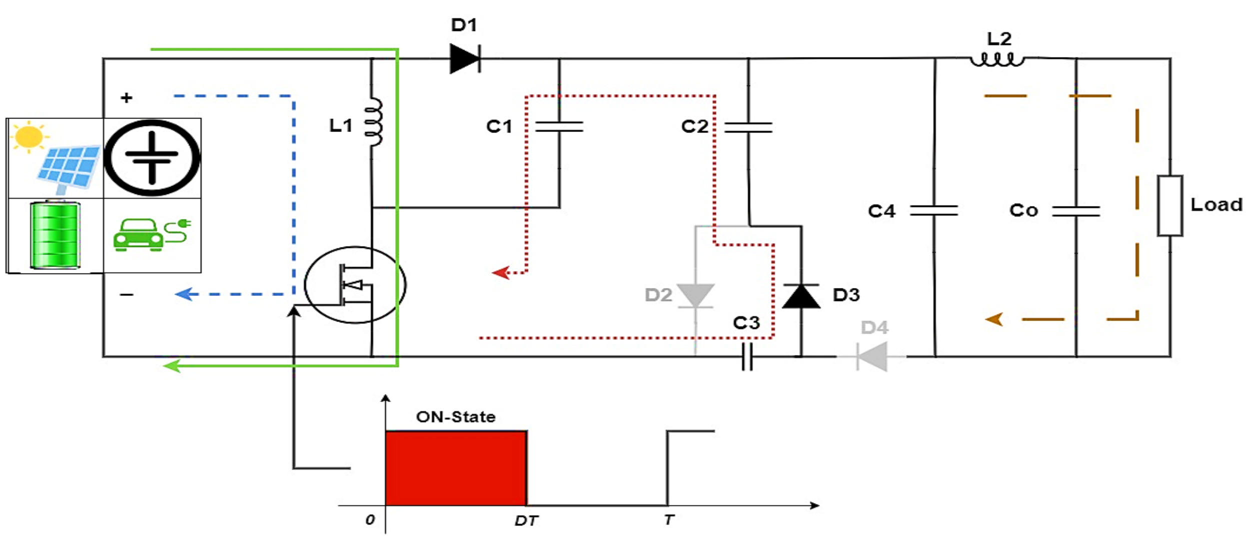


Figure (3.4). SC Luo converter when S1 is ON.

As the switching device is in an off state in the next period, as shown in Figure (3.5), inductors L_1 discharge, making a series circuit with capacitors C_1 and C_2 and diode D_2. Capacitor C_1 is draining while capacitor C_2 is charging, compared to the previous operating mode. Capacitor C_4 takes a charge via the input supply as capacitor C_3 discharges the charge across diode D_4. The brief description of this specific operational condition is (KT < t < T).

$$(3.5) V_{in} = V_{L1} - V_{C1} + V_{C2}$$

$$(3.6) V_{in} = V_{L1} - V_{C1} + V_{C4} - V_{C3}$$

$$(3.7) V_{C4} = V_{L2} + V_{O}$$

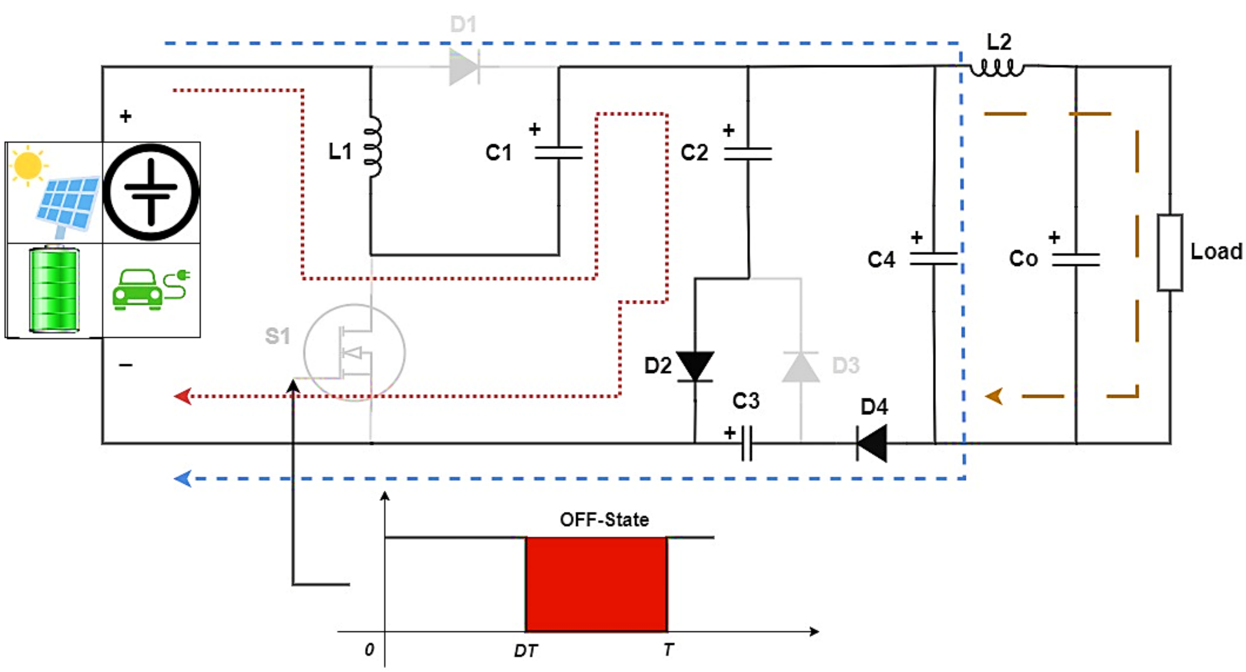


Figure (3.5). SC Luo converter when S1 is OFF.

All semiconductor devices are regarded as disconnected in a discontinuous conduction mode, as shown in Figure 3.6. Because diodes D_2, D_3, and D_4 are off, capacitors C_2 and C_3 are bypassed. Capacitor C_2's voltage falls into its end load. This voltage eventually drops to zero after a brief time.

One of the components that helps to smooth the output current is the filtered inductor, L_2. Interestingly, after about five times the output RC circuit's time constant, the current flowing across this inductor reaches zero.

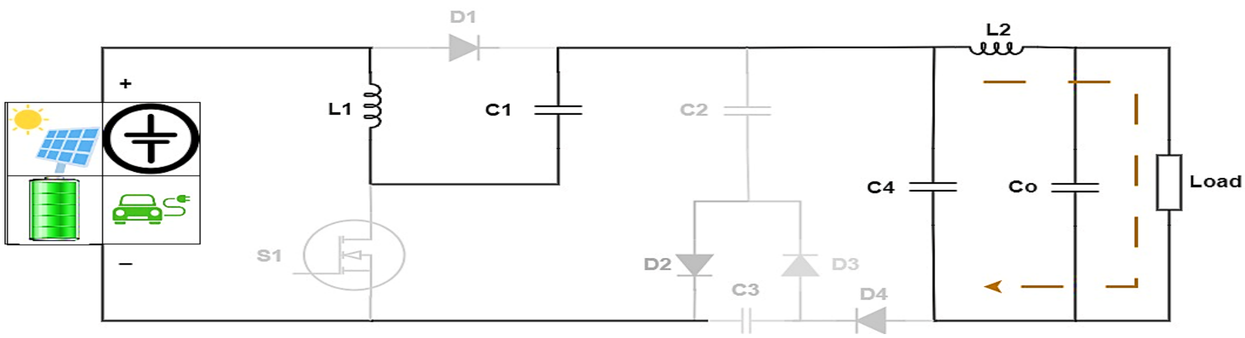


Figure (3.6). SC Luo converter in discontinuous conduction mode.

Voltage of the inductors L_1, by incorporating Equations (3.2) and (3.5). The voltage passing across capacitor C_3 is as follows:

$$V_{L1} = 2V_{in} - V_{C2} \tag{3.8}$$

According to the second voltage balancing rule that applies to inductors, the mean voltage across the inductor in a switched power conversion circuit must be almost zero. This means that for inductor L_1, this can be stated as follows:

$$\int_0^{KT} V_{\text{in}}\, dt + \int_{KT}^{T} (2V_{in} - V_{C2})dt = 0 \tag{3.9}$$

As a result, the voltage in capacitor C_2 can be determined as follows:

$$V_{C2} = \frac{2-K}{1-K} V_{\text{in}} \tag{3.10}$$

By taking a look at Figure (3. 4) :

$$V_{C1} = V_{C2} - V_{C3} \tag{3.11}$$

Considering that Equations (3.2) and (3.10) yield the values of V_{C1} and V_{C2}:

$$V_{C3} = \frac{2-K}{1-K} V_{\text{in}} - V_{\text{in}} = \frac{1}{1-K} V_{\text{in}} \quad (3.12)$$

According to Figure (3.5):

$$V_{C4} = V_{C2} + V_{C3} = \frac{2-K}{1-K} V_{\text{in}} + \frac{1}{1-K} V_{\text{in}} = \frac{3-\text{K}}{1-K} V_{\text{in}} \quad (3.13)$$

The initial assumption is that the mean voltage flowing across an inductor in a steady-state operating mode is zero. This can, therefore, be stated as follows:

$$V_{L2} \cdot K = -V_{L2} \cdot (1 - K) \quad (3.14)$$

Thus, V_{C4} is equal to the output voltage, V_{out}, and

$$V_{out} = \frac{3-\text{K}}{1-K} V_{\text{in}} \quad (3.15)$$

3.5 Conversion Efficiency

The efficiency of the power conversion circuit is a further vital factor. As such, it is necessary to compute switching and dynamic power losses for every element in a circuit to produce an accurate power loss equation. The internal resistances associated with the components, which are usually insignificant under optimal operating circumstances, are the primary source of dynamic losses. However, these small resistances can occasionally result in significant dynamic losses in practical circumstances. The root mean square (RMS) current for every element is crucial. In semiconductor components, switching losses become associated with the crossing and overlapping regions throughout the on/off operations. In an ideal situation, voltage and current waveforms should quickly transition between the highest and lowest sides, potentially exhibiting minimal portions of the voltage and current. However, those waveforms require a limited time to reach zero or achieve their highest values. Because of this, when switching occurs, current and voltage levels coexist, leading to phenomena that are known as switching losses. The latest model of power semiconductors has lower internal resistances to minimize dynamic losses, which in turn results in lower dynamic losses. Soft switching approaches, such as zero voltage and zero current switching or zero voltage and zero current transition, are advised to reduce switching losses. The process for determining the losses that the circuit components experience is outlined in the next section.

3.5.1. Switch Losses

After obtaining the gain formula, the relationship between the input and output currents can be calculated as follows:

$$P_{\text{in}} = P_{out} \tag{3.16}$$

$$V_{\text{in}} I_{\text{in}} = V_{out} I_{out} \rightarrow \frac{I_{out}}{I_{\text{in}}} = \frac{V_{\text{in}}}{V_{out}} \tag{3.17}$$

$$\frac{I_{out}}{I_{\text{in}}} = \frac{1-K}{3-K} \rightarrow I_{\text{in}} = \frac{3-K}{1-K} I_{out} \tag{3.18}$$

When the switch is activated, the current passing across it can be calculated as follows:

$$I_{SW} = I_{L1,on} + I_{C1,on} \tag{3.19}$$

$I_{L1,on}$indicates the current flowing through inductor L_1 when the switch is on, whereas I_{SW} indicates the current flowing through the switch. In the same way, $I_{C1,on}$ denotes the current flowing through capacitor C_1 while the switch is in the on position.

The RMS current value must be calculated to ascertain the switch's dynamic losses. The integral technique is traditionally used to determine a signal's RMS value.

$$I_{\text{SW},rms} = \sqrt{\frac{1}{T}\int_0^{KT} \left(I_{L1} + I_{C_1,on}\right)^2 dt} \tag{3.20}$$

By considering r_{on} as the resistance of the switch, the power $P_{r_{on}}$ of dynamic loss is calculated as follows:

$$P_{r_{on}} = r_{on}\, I_{S,rms}{}^{2} \tag{3.21}$$

The voltage V_{sw} through the switch during the switching operation, the switching frequency (f_{sw}), and the switching current (I_{sw}) in the switching device, all must be considered to estimate the switching losses. Usually, the datasheet for the switch is utilized to get these values. For the proposed converter, the following formula is then used to calculate switching losses P_{SW}:

$$V_{sw} = V_{C2} - V_{C1}$$

$$P_{SW} = \frac{1}{2} I_{sw} V_{sw} = f_s (V_{C2} - V_{C1}) \tag{3.22}$$

Both dynamic and switching losses are included in the total power losses P_{SL} for the switch, which is written:

$$P_{\mathrm{Switch}} = 2 \cdot P_{SW} + P_{r_{on}} \tag{3.23}$$

Since two switching operations occur during each switching duration, switching losses must be calculated as twice the switch loss.

3.5.2. Diodes Losses

It is essential to ascertain the RMS currents passing through each switch to calculate the dynamic losses for each one:

$$I_{D_1} = I_{C1,on} + I_{C2,on} \rightarrow P_{Dy,\mathrm{D1}} = R_{\mathrm{on},D_1}\ I_{D_1}{}^{2}$$

$$= R_{\mathrm{int},D_1} \times \left(\sqrt{\frac{1}{T}\int_0^{KT} \left(I_{C2,on} + I_{C3,on}\right)^2 dt} \right)^2 \tag{3.24}$$

$$I_{D_2} = I_{C2,\,\text{off}} \rightarrow P_{Dy,D_2} = R_{\text{int},D_2}\, I_{D_2}^2$$

$$= R_{\text{int},D_2} \times \left(\sqrt{\frac{1}{T}\int_0^{KT} \left(I_{C2,0ff}\right)^2 dt}\right)^2 \tag{3.25}$$

$$I_{D_3} = -I_{C2,\,\text{on}} \rightarrow P_{Dy,D_3} = R_{\text{int},D_3}\, I_{D_3}{}^2$$

$$= R_{\text{int},D_3} \times \left(\sqrt{\frac{1}{T}\int_0^{KT} \left(-I_{C2,on}\right)^2 dt}\right)^2 \tag{3.26}$$

$$I_{D_4} = -I_{C3,0ff} \rightarrow P_{Dy,D_4} = R_{\text{int},D_4}\, I_{D_3}{}^2$$

$$= R_{\text{int},D_4} \times \left(\sqrt{\frac{1}{T}\int_0^{KT} \left(-I_{C3,off}\right)^2 dt}\right)^2 \tag{3.27}$$

This series of formulas makes use of many parameters. the internal resistance values for diodes are represented by $R_{\text{int},D_\text{x}}$ and forward voltage are shown by V_{D_x}. The dynamic loss formula for the diodes, P_{Dy,D_x}, is related to RMS current of the diodes.

The next step is to calculate the switching losses of the diodes, which requires accounting for the average current of the diodes. The average current of D_x is denoted by I_{D_3} in the following equations.

$$P_{SW,D_1} = V_{F_1} I_{D_1} = V_{D_1} \frac{1}{T}\int_{KT}^{T} \left(I_{C1,on} + I_{C2,\,\text{on}}\right) dt \tag{3.28}$$

$$P_{SW,D_2} = V_{D_2} I_{D_2} = V_{D_2} \times \int_{KT}^{T} \left(I_{C2\ \text{off}}\right) dt \tag{3.29}$$

$$P_{SW,D_3} = V_{D_3} I_{D_3} = V_{D_3} \times \int_{KT}^{T} \left(-I_{C2,\,\text{on}}\right) dt \tag{3.30}$$

$$P_{SW,D_4} = V_{D_4} I_{D_4} = V_{D_4} \times \int_{KT}^{T} \left(-I_{C3,\,\text{off}}\right) dt \tag{3.31}$$

The total losses in diodes can be described in the following equations:

$$P_{SW,\text{total}} = P_{SW,D_1} + P_{SW,D_2} + P_{SW,D_3} + P_{SW,D_4} \quad (3.32)$$

$$P_{Dy,\text{total}} = P_{Dy,\text{D1}} + P_{Dy,D_2} + P_{Dy,D_3} + P_{Dy,D_4} \quad (3.33)$$

$$P_{\text{Diodes}} = P_{SW,\text{total}} + P_{Dy,\text{total}} \quad (3.34)$$

Where $P_{SW,\text{total}}$ is the total switching losses, and $P_{Dy,\text{total}}$ is the total dynamic losses in diodes.

3.5.3. Inductors losses

In the steady-state operating mode, the average current of the capacitors is zero. Consequently, the following formula can be used to determine the current of the inductors:

$$I_{L_1} = \frac{I_{in}}{2} = \frac{3-K}{2(1-K)} I_{\text{out}} \quad (3.35)$$

The internal resistance of inductors L_1 and L_2 are represented by R_{int,L_1} and R_{int,L_2}, and the dynamic losses connected to these relative inductors are shown by P_{Dy,L_1} and P_{Dy,L_2}.

$$P_{Dy,L_1} = R_{int,L_1} {I_{L_1}}^2 = R_{on,L_1} \left(\frac{3-K}{2(1-K)}\right)^2 {I_{out}}^2 \quad (3.36)$$

$$P_{Dy,L_2} = R_{int,L_2} {I_{L_2}}^2 = R_{on,L_2} \left(\frac{3-K}{2(1-K)}\right)^2 {I_{out}}^2 \quad (3.37)$$

The total losses in inductors $P_{Inductors}$ can be described in the following equations:

$$P_{Inductors} = P_{Dy,L_1} + P_{Dy,L_2} \quad (3.38)$$

3.5.4. Capacitors Losses

In a DC-DC converter, capacitors cause power losses due to charging/discharging cycles, leakage currents, and switching transients. These losses can be calculated as follows:

3.5.4.1. Switching Losses Due to Parasitic Capacitance

When a semiconductor switch (MOSFET, IGBT, etc.) turns on/off, parasitic capacitance stores and dissipates energy in each cycle. The energy loss per switching cycle is:

$$E_{parasitic} = \frac{1}{2} C_{parasitic} V_C^2 \quad (3.39)$$

Where $E_{parasitic}$ is energy loss per switching cycle (J), $C_{parasitic}$ is parasitic capacitance (F) and V is Voltage across the capacitor (V).

The total power loss over the switching period is:

$$P_{parasitic} = f_s \times E_{parasitic} = \frac{1}{2} C_{parasitic} V_C^2 \quad (3.40)$$

Where $P_{parasitic}$ is power loss due to parasitic capacitance (W) and fs is switching frequency (Hz).

3.5.4.2. Leakage Losses in Parasitic Capacitors

Leakage current flows through parasitic capacitance even when the switch is off, causing static power loss:

$$P_{leakage} = V_c \times I_{leakage} \quad (3.41)$$

Where $I_{leakage}$ is Leakage current (A).

3.5.5 The Overall Power Loss and Efficiency

The following is the formulation of the complete power loss equations into the proposed converter, which includes the capacitors' insignificant internal resistance:

$$P_{Total\ Loss} = P_{Switch} + P_{Diodes} + P_{\text{Inductors}} + P_{Capacitors} \tag{3.42}$$

Therefore, the equation for efficiency (η) for the proposed converter can be expressed in the following manner:

$$\eta = \frac{P_{out}}{P_{out}+P_{Total\ Loss}} * 100 \tag{3.43}$$

3.6 Voltage Stress

When considering each part's stability and the converter's dependability under various operating conditions, such as varied input voltages and duty ratios, the evaluation of voltage stress on the switch and other semiconductor elements is essential. The following part discusses and shows the voltage stress on the diode (D_1) and the switch. The following equations can be used to determine the voltage stress on switch S_1 :

$$V_S = -V_{C1} + V_{C2} = -V_{\text{in}} + \frac{2-\text{K}}{1-K}V_{\text{in}} = \frac{1}{1-K}V_{\text{in}} \tag{3.44}$$

This formula shows that the voltage stress across the switch expands with a rise in the input voltage or duty ratio. The following Equations can be used to find the voltage through diode D_1 in OFF operation.

$$V_{D1} = V_{L1} - V_{C2} = 2V_{in} - V_{C2} - V_{C2}$$

$$= 2(V_{in} - \frac{2-K}{1-K}V_{\text{in}}) = \frac{2}{1-K}V_{\text{in}} \tag{3.45}$$

This simple equation shows that variations in the duty ratio do not affect the voltage flowing across diode D_1, which is exclusively dictated by the input supply voltage, V_{in}

3.7 The current ripple and the voltage ripple

The variations between the maximum and minimum inductor currents can be used to calculate the ripple in the inductor's current. Consequently, the simplified phrase includes the inductor voltage in an operating mode. Additionally, the variation in the maximum and minimum capacitor voltages can be used to compute the ripple in capacitor voltage. As a result, the capacitor current is included in an operating mode in the shortened term. The ripples in the capacitor voltage and the inductor current are as follows:

$$\Delta i_{L_1} = \frac{DV_{in}}{L_1 f_s}, \Delta i_{L_2} = \frac{DV_{in}}{(1-D)L_2 f_s} \quad (3.46)$$

$$\Delta v_{C_1} = \frac{DV_O}{(1-D)RC_1 f_s}, \Delta v_{C_2} = \frac{V_O}{RC_2 f_s}, \Delta v_{C_o} = \frac{DV_O}{C_O f_s} \quad (3.47)$$

3.8 Controller Design

Applying a PID controller can yield benefits for a step-up converter, including increased transient response, greater steady-state accuracy, and flexibility to accommodate a range of operating situations. Contemporary control design devices, modeling, and systematic tuning techniques simplify the relatively complicated process of tuning PID parameters.

This guarantees accessibility during the tuning procedure and promotes the best possible converter functionality across various uses. The difference between the intended reference input (V ref) and the actual voltage that is output (V out) of the converter, as shown in Figure (3.7) and time (t) is represented as the error signal, or e(t):

$$e(t) = V_{\text{ref}} - V_{\text{out}} \quad (3.48)$$

The control signal input represents the duty cycle ($d(t)$) of the converter's switch at time t. The equation for the PID controller is as follows:

$$d(t) = K_p e(t) + K_i \int_0^t e(\tau)d\tau + K_d \frac{de(t)}{dt} \tag{3.49}$$

The proportional gain, shown by K_p, it determines how quickly the controller responds to the current error signal by increasing it straight. By integral the error signal over time, K_i, The integral gain accumulates the error over time to remove steady-state errors. The derivative gain, or K_d, It lessens overshooting and improves system stability by accounting for the rate at which the error signal changes to predict future changes. The definition of the error signal, e(t), is given above $\int_0^t e(\tau)$. The error signal's integral value over time is indicated by dt, and its derivative about time is denoted by $\frac{de(t)}{dt}$.

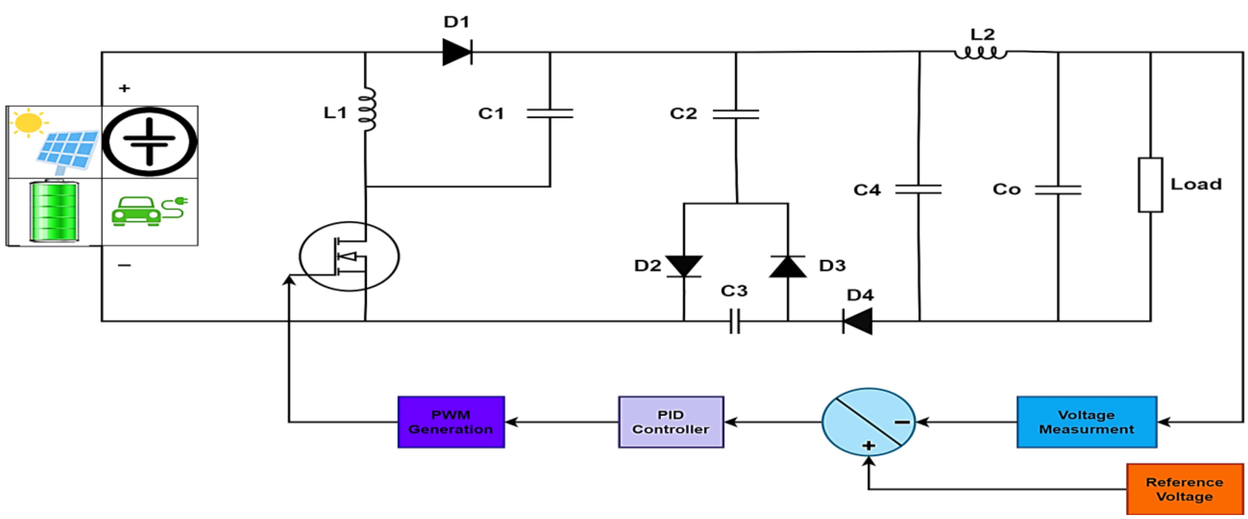


Figure (3.7). The proposed converter's simple control process approach.

3.9 The proposed modified POSLLC model parameters at K=0.5.

The switching frequency is 100KHZ, its inductor value can be calculated by the current ripple equation. Let assume the ripple current is between (0.2- 0.4). Figure (3.8) shows the simulated model of the proposed modified POSLLC at duty cycle =0.5.

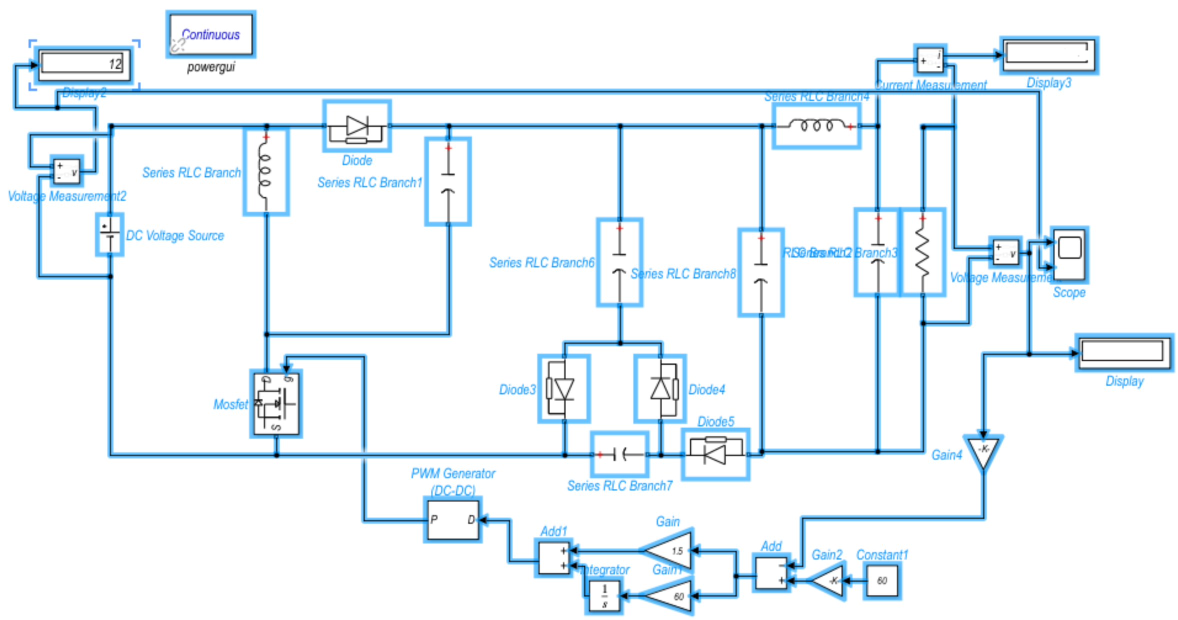


Figure (3.8). The simulated model of the proposed modified POSLLC at D=0.5

Let R= 1000 Ω

Input voltage =12 V

Duty cycle =0.5

The output current value is $Io = \frac{Vo}{R} = 0.06\ A$

$\Delta IL_1 = \frac{V_{in}}{L_1} \times KT$ whereas $T = 1/f$

$T = 1/100000$

$L_1 = \frac{V_{in}}{\Delta IL_1} \times KT \rightarrow L_1 = 2.5\ mH$

From eq.(3.46) $L_2 = \frac{0.5 \times 12}{(1-0.5)\times 0.024 \times 100 \times 10^3} = 5\ mH$

Using eq. (3.47) to calculate the values of the capacitors

Voltage ripple can be obtained as Δvc_1 is 1% of the output voltage equals 0.6.

$$C_1 = \frac{KVo}{(1-K)R\ Fs\ \Delta vc_1} \rightarrow \qquad C_1 = 1.33\ \mu F$$

Let assume the voltage ripple is 2% of the output voltage, thus Δvc_2 = 1.2 ,

using eq.(3.47) to obtain the value of boost capacitor equals: $C_2 = 6.66\ \mu F$.

then the output capacitance equals: $C_O = 20 \times 10^{-4} F$,the table below shows the parameters of modified single cell circuit at K=0.5.

Table (3.2) :The Proposed Modified Single Cell Circuit Parameters

Parameter's name	Symbol	Value
Input voltage	Vin	12 V
Output voltage	Vo	60 V
Inductors	L_1,L_2	2.5mH , 5mH
Capacitors	C_1,C_2,C_3,C_4,C_o	1.33μF,6.66μF, 20×10^{-4} F
switching frequency	F s	100KHz
Load resistance	R	1000
Duty cycle	K	0.5

3.10 The Multistage Modified Positive Output Super-Lift Luo Converter

The Multistage Modified Positive Output Super-Lift Luo Converter is a highly advanced power conversion technology that provides exceptional voltage gain, and reliability. The use of this technology in diverse contemporary electronic systems highlights its significance in enhancing the functionalities of power electronics. The multistage switched capacitor cell technology employs a series of capacitors to gradually amplify the voltage. Each step progressively amplifies the voltage, leading to a far greater total amplification than what a single-stage converter can do.

Now the mathmatical analysis of the proposed modification ,

When the switch is ON

$$V_{L1} = L_1 \cdot \frac{di_{L1}}{dt} = V_{in} \quad (3.50)$$

$$V_{C1} = V_{L1} = V_{in} \quad (3.51)$$

$$V_{\text{in}} = V_{C2} - V_{C3} \quad (3.52)$$

$$V_{C4} = V_{L2} + V_{C5} - V_{C6} \quad (3.53)$$

$$V_{C7} = V_{L3} + V_{Co} \quad (3.54)$$

When the switch is off

$$(3.55) V_{in} = V_{L1} - V_{C1} + V_{C2}$$

$$V_{C2} = V_{C4} - V_{C3} \quad (3.56)$$

$$V_{C4} = V_{L2} + V_{C5} \quad (3.57)$$

$$V_{C5} = V_{C7} - V_{C6} \quad (3.58)$$

$$V_{C7} = V_{L3} + V_{Co} \quad (3.59)$$

Voltage of the inductors L_1, by incorporating Equations (3.51) and (3.55). The voltage passing across capacitor C_3 is as follows:

$$V_{L1} = 2V_{in} - V_{C2} \quad (3.60)$$

According to the second voltage balancing rule that applies to inductors, the mean voltage across the inductor in a switched power conversion circuit must be almost zero. This means that for inductor L_1, this can be stated as follows:

$$\int_0^{KT} V_{\text{in}}\, dt + \int_{KT}^{T} (2V_{in} - V_{C2}) dt = 0 \quad (3.61)$$

As a result, the voltage in capacitor C_2 can be determined as follows:

$$V_{C2} = \frac{2-k}{1-k} Vin \quad (3.62)$$

Considering that equations (3.51) and (3.62) yield the values of V_{C1} and V_{C2}:

$$V_{C3} = V_{C2} - V_{in} = \frac{1}{1-k} V_{in} \quad (3.63)$$

from eq. (3.56), we can get

$$V_{C4} = V_{C2} + V_{C3} = \frac{3-k}{1-k} V_{in} \tag{3.64}$$

The initial assumption is that the mean voltage flowing across an inductor in a steady-state operating mode is zero. This can, therefore, be stated as follows:

$$V_{L2} \cdot K = -V_{L2} \cdot (1 - K) \tag{3.65}$$

Thus

$$V_{C5} = V_{C4} = \frac{3-k}{1-k} V_{in} \tag{3.66}$$

Subtitue eq (3.66) in eq (3.53)

$$V_{C6} = \frac{9-3k}{1-k} V_{in} \tag{3.67}$$

From eq.(3.58) ,

$$V_{C7} = V_{C5} + V_{C6} = \frac{12-4k}{1-k} V_{in} \tag{3.68}$$

The initial assumption is that the mean voltage flowing across an inductor in a steady-state operating mode is zero. This can, therefore, be stated as follows:

$$V_{L3} \cdot K = -V_{L3} \cdot (1 - K) \tag{3.69}$$

Thus $V_{C7} = V_{Co}$

The output voltage equation for double cell modification is:

$$V_{out} = \frac{12-4k}{1-k} V_{in} \tag{3.70}$$

3.10.1 Proposed Modified POSLLC based on multi-switched capacitor cell parameters

In this modification , we repeated the switched capacitor cell twice and we got a high transfer voltage gain at duty cycle = 0.5 . the figure below shows the circuit configruation .

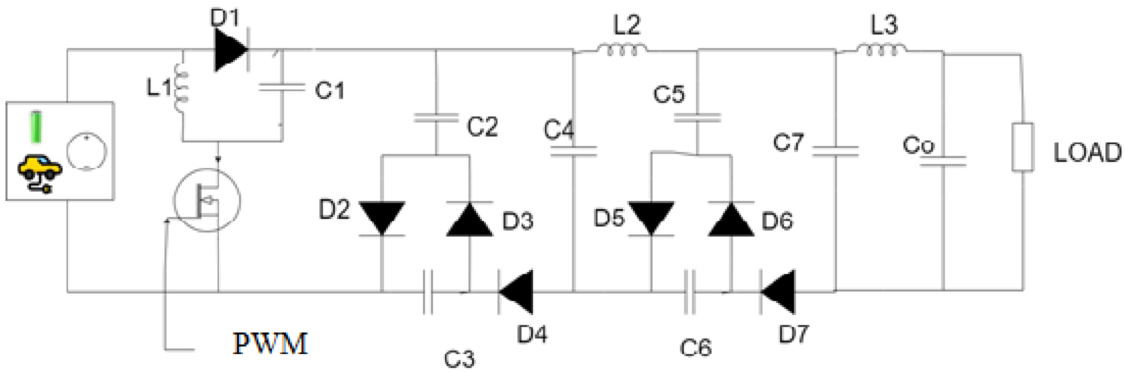


Figure (3. 9). The multi Switched Capacitor Cell Modification

Figure (3.10) shows the simulated model of modified POSLLC based on multi switched capacitor cell .

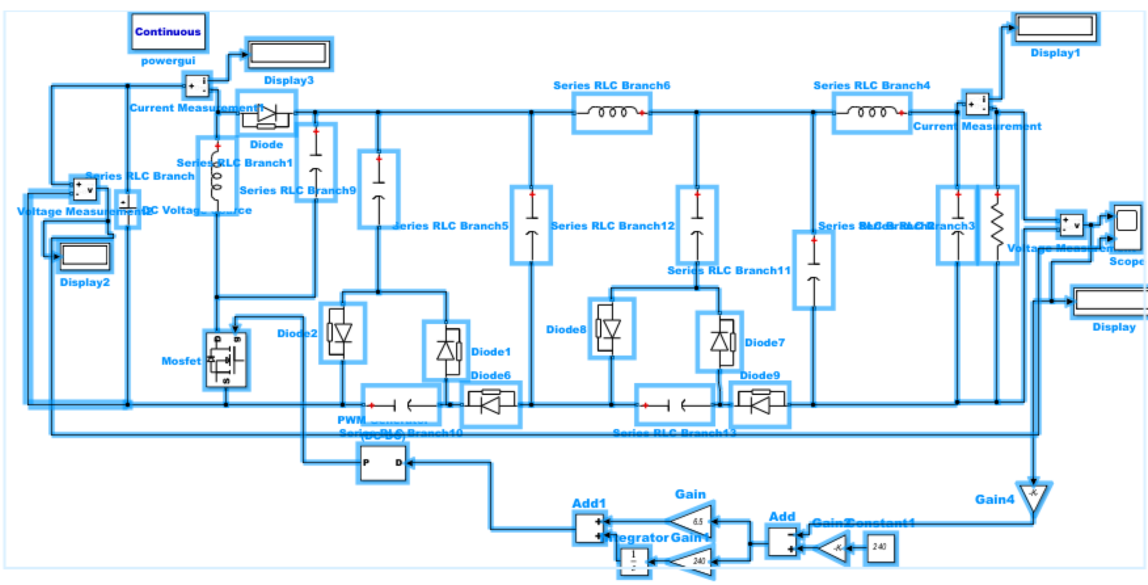


Figure (3.10). The simulated model of proposed modified multi-s.c

The given parameters are :

Duty cycle = 0.5

Input voltage Vin =12V
Switching frequency Fs = 100 KHZ
Load resistance R=1 KΩ
The output current is $Io = 0.24\ A$
Using this eq.(3.46) $\Delta IL_1 = \frac{V_{in}}{L_1} \times KT$
whereas $T = 1/f$ then $T = 1/100000$
from eq.(3.46) ,we get the value of $L_1 = 8.33 \times 10^{-4} H$
$L_2 = L_3 = 1.667\ mH$
To obtain the values of the capacitors ,we assume voltage ripple is 1 % .
$\Delta vc_1 = 0.01 \times 240 = 2.4$
By using equations (3.47), Then $C_1 = 1\mu f$
And the value of $C_{cell} = 1\ \mu f$,While the value of the output capacitance $C_o = 20 \times 10^{-4} f$,The parameters are shown in table below .

Table (3.3): The Parameters of Proposed Modified Multi Switched Capacitor Cell Circuit

Parameter's name	Symbol	Value
Input voltage	V_{in}	12 V
Output voltage	V_o	240 V
Inductors	L_1,L_2,L_3	$8.33 \times 10^{-4} H$,1.667mH
Capacitors	C_1,C_{cell},C_o	1µF, 1µF, 20×10^{-4} F
switching frequency	F_s	100KHz
Load resistance	R	1000
Duty cycle	K	0.5

CHAPTER FOUR

Chapter four

Simulation Results and Discussions

4.1 Introduction

The proposed converter was simulated using MATLAB/Simulink. It shows many output levels across various input voltages and output loads. Measurements of current and voltage are conducted on the circuit component. The simulation results were subsequently compared with theoretical calculations to evaluate the alignment of voltage and current characteristics with both theoretical and simulation-derived conclusions. The results demonstrate significant consistency by demonstrating the connection within mathematical analysis.

4.2 Simulation Results for Conventional POSLLC and The Proposed Modified POSLLC

The simulation results of the proposed conventional POSLLC DC-DC converter indicated a voltage gain of three times when the input voltage was 12 volts and the duty cycle was 0.5, resulting in an output voltage of 36 volts.

Figure (4.1) contrasts the voltage gain of the proposed converter and the conventional converter. This graphic shows that the proposed converter has much higher gain levels. when the duty cycle (K) value is 0.9, the proposed converter's gain is 21 times the input sources, while a conventional converter's gain reaches only 10 times the input sources, as the figure plainly shows.

The high gain values of proposed converter make it ideal for low-voltage uses, including fuel cells, batteries, and solar systems. It is well known that these specific clean energy sources provide comparatively low DC voltages. To utilize such sources for tasks such as powering a DC motor or linking to the grid, the voltage produced must first be raised to the necessary level for the utilized load. Obtaining the current and voltage levels for different components is feasible, including the times the switch toggles on and off. The current and voltage waves of the inductors are shown in Figure (4.2). Furthermore, the voltage waves for the capacitors and diodes, respectively, are shown in Figure (4.3),(4.4).

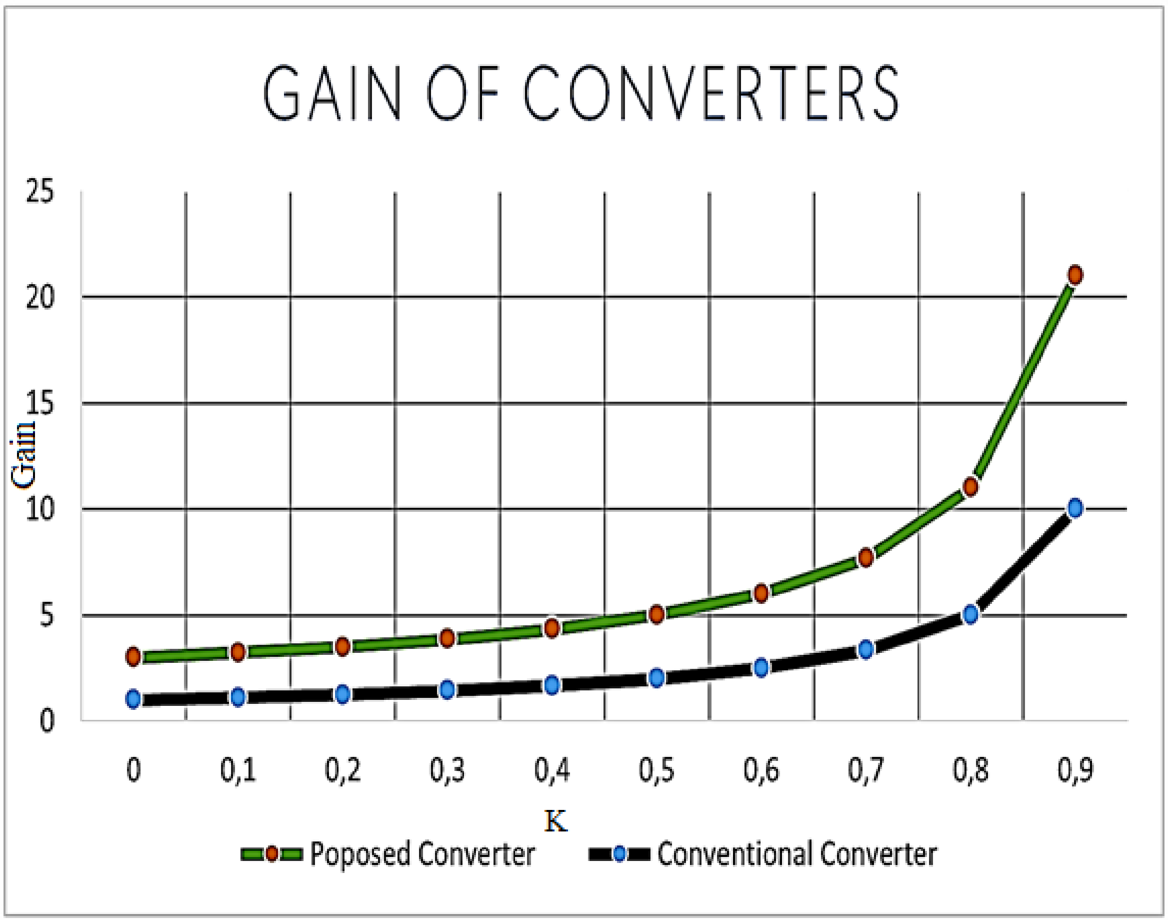
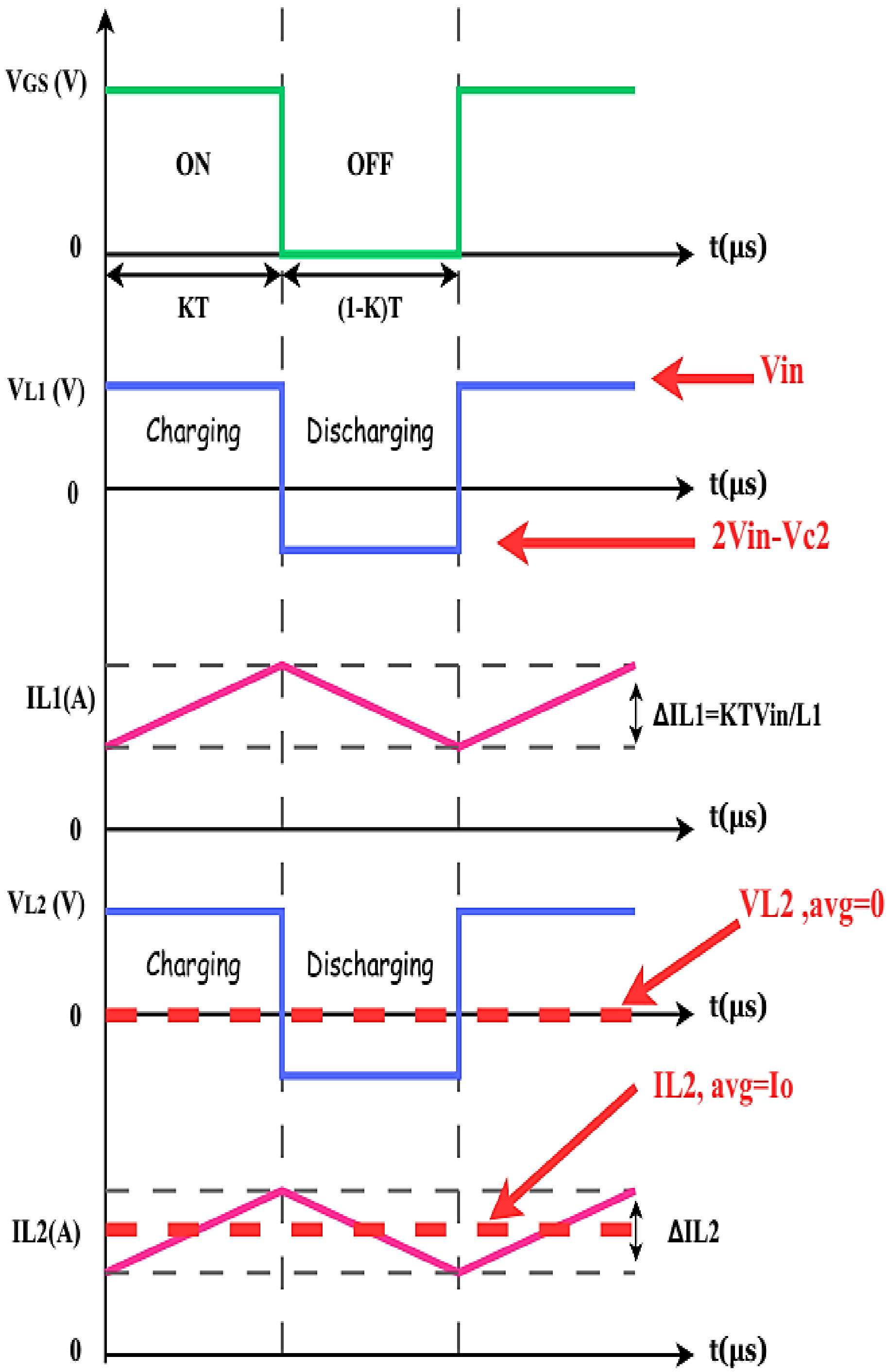


Figure (4.1). Gain curves for 0.1 < K< 0.9 for the proposed modified POSLLC and conventional POSLLC converter.



Figure(4.2) . Inductors Voltage and current waves of proposed modified POSLLC .

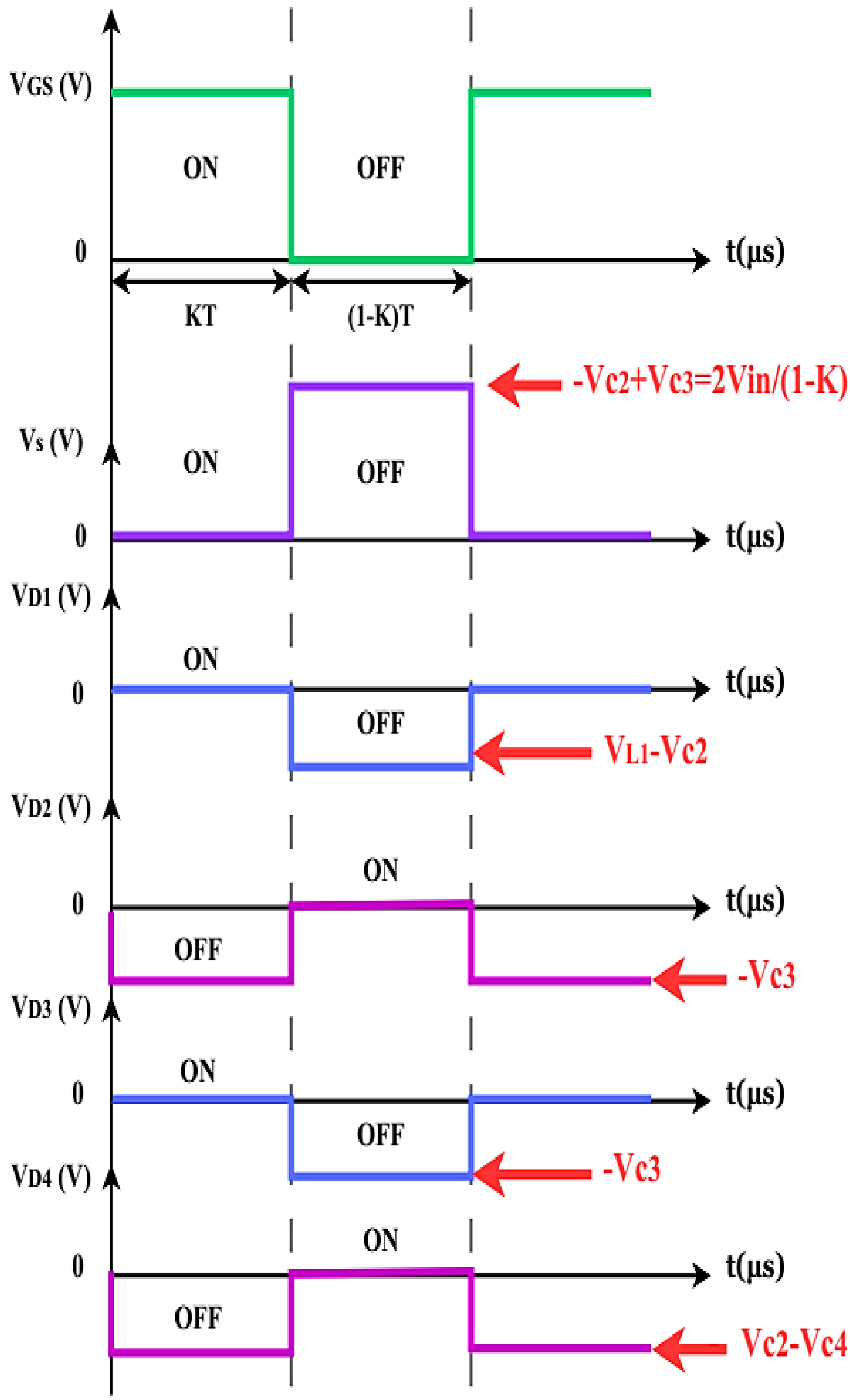


Figure (4.3). Diodes Voltage waves of Proposed modified POSLLC.

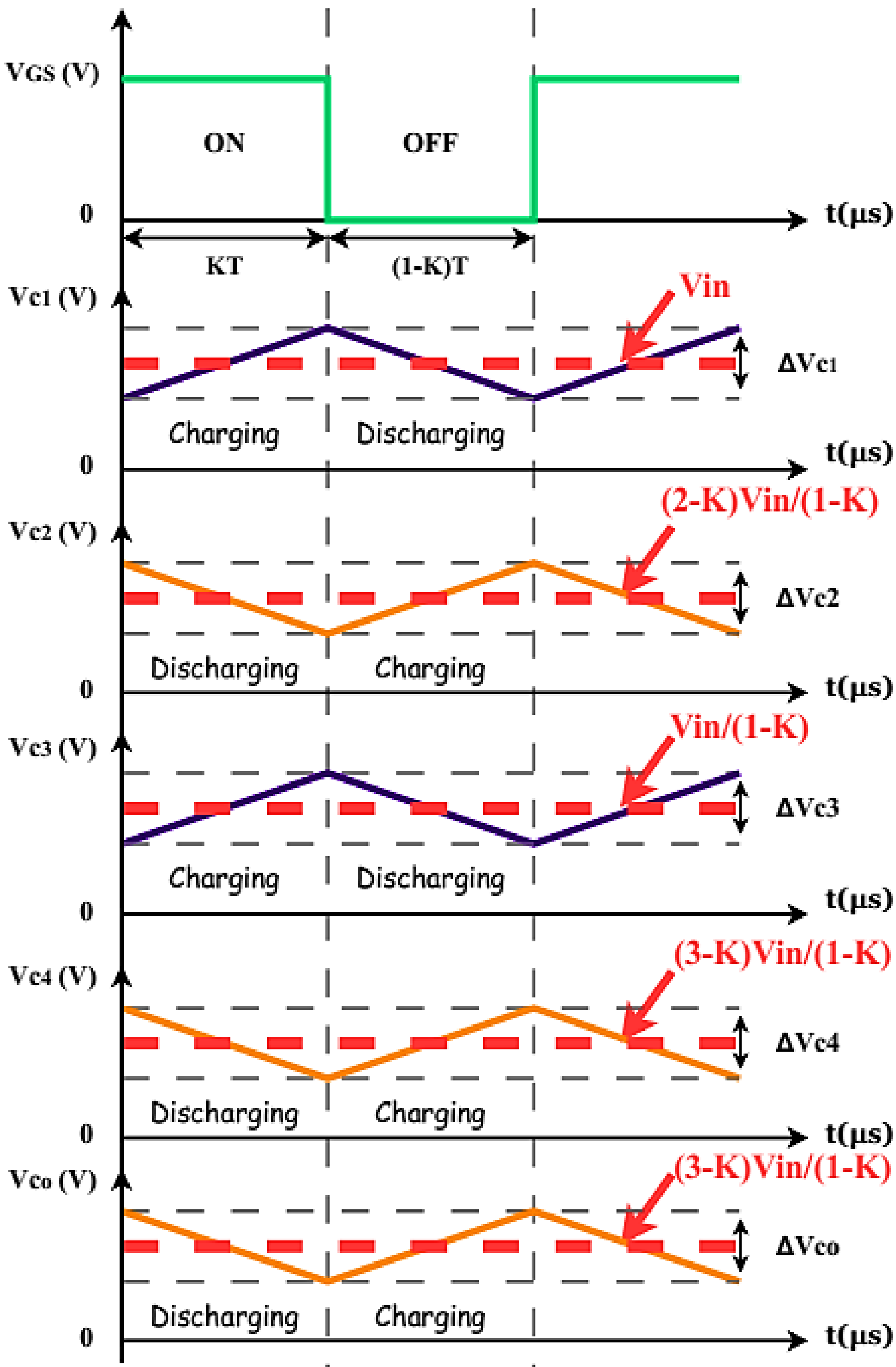


Figure (4.4). Capacitors Voltage waves of proposed modified POSLLC

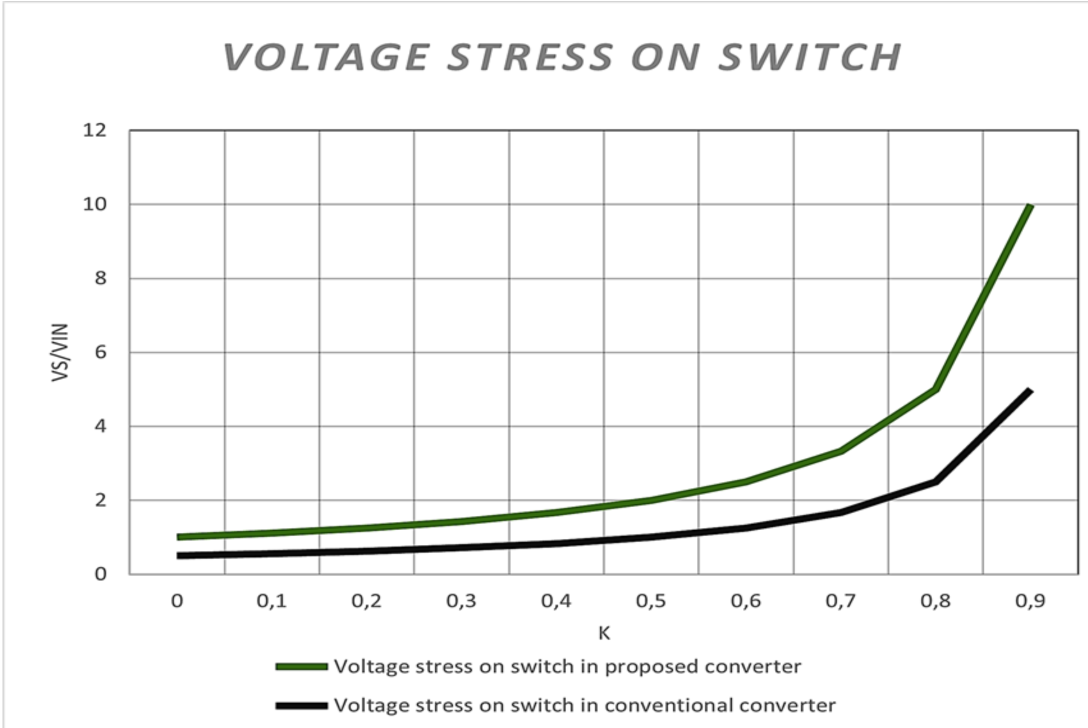


Figure (4.5). Switch Voltage Stress of proposed modified POSLLC

Figures (4.5) illustrate the voltage stress of the proposed modified converter with conventional converter on the switch.

Figure (4.6) shows a diagram of The voltage stress of the traditional converter and proposed converter is also shown in the figure. The drawing makes it clear that the diode in the suggested converter has a higher voltage stress value than the traditional converter.

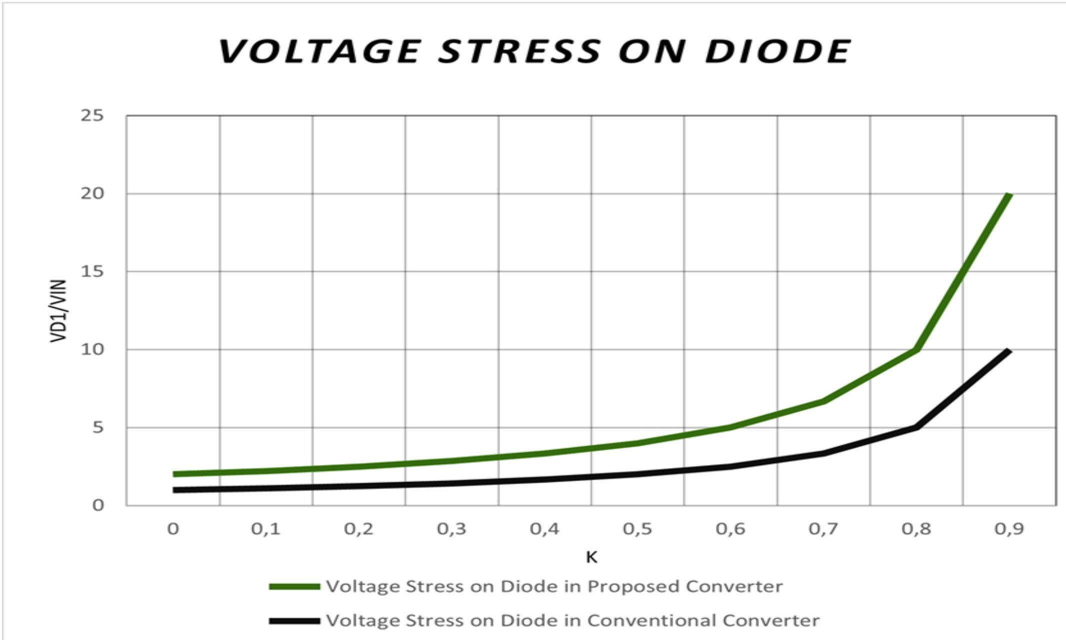


Figure (4.6). Diode Voltage Stress of proposed modified POSLLC

Figure (4.7) illustrates the input and output voltages. With the input voltage set to 12 VDC, the load generates approximately about 60 VDC, which aligns with expectations. It is crucial to remember that accurate voltage gain computations require taking voltage dips across all components into account.

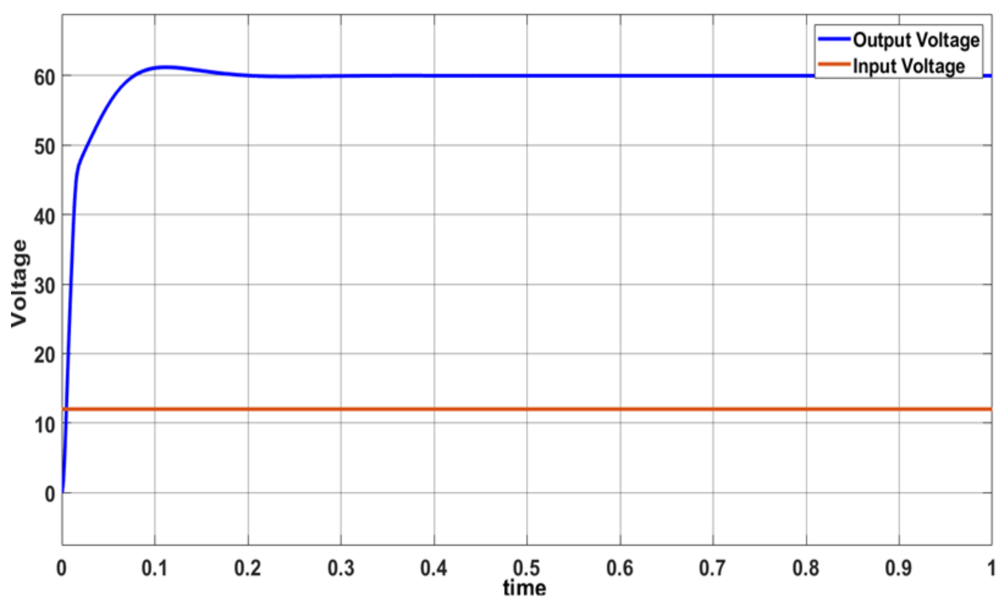


Figure (4.7). Input and output voltage at K=0.5 of proposed modified POSLLC.

Figure (4.8) confirms the accuracy of the voltage values over diodes based on a mathematical analysis of the converter, as shown in Figure (4.4) . These updated figures show that just one diode (D2, D3, and D4) must be in the "on" mode at any specified switching period due to its asynchronous nature. This finding confirms that the circuit performance is consistent with the ideas shown in Figure (4.4).

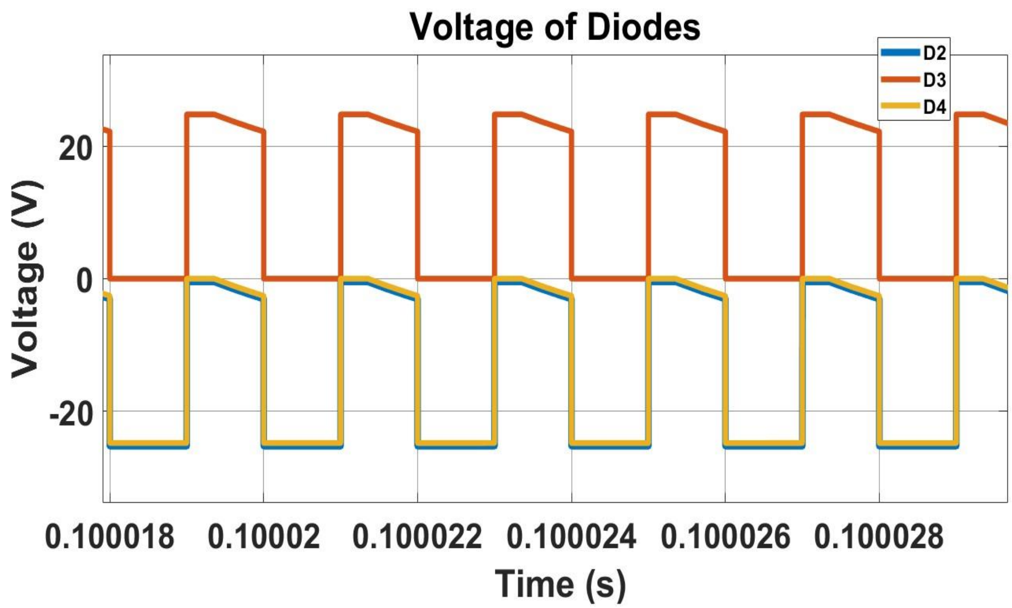


Figure (4.8). Voltage across diodes D2 to D4 of proposed modified POSLLC at K= 0.5.

In figure (4.9), The operational modes of switch S and diode D4 are shown. It was expected that these parts would function asynchronously, which means that diode D4 must be disabled if the switch was activated and the reverse is true. Figure (4.4) clearly illustrates these asynchronous actions, and the outcomes match the predictions shown in those figures.

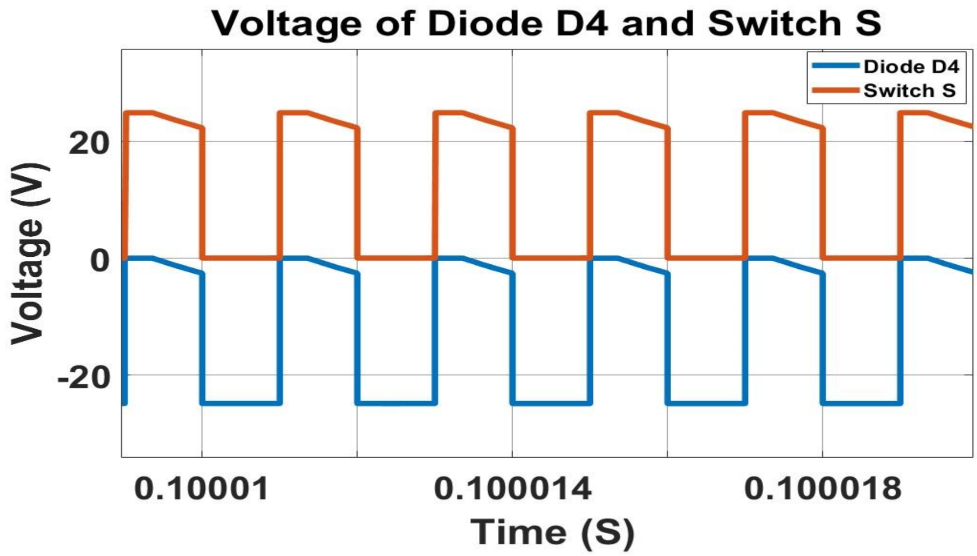


Figure (4.9). Voltage across diodes D4 and Switch S of proposed modified POSLLC at K= 0.5.

Figure (4.10) shows the current waveforms of switch S and inductor LI. As expected, the input current for the inductors showed a good state, oscillating between 0.08 and 0.12 A from peak to peak. During the switching occurrences, no notable undershoots or overshoots were noted. Switch S's present switching state was remarkable.

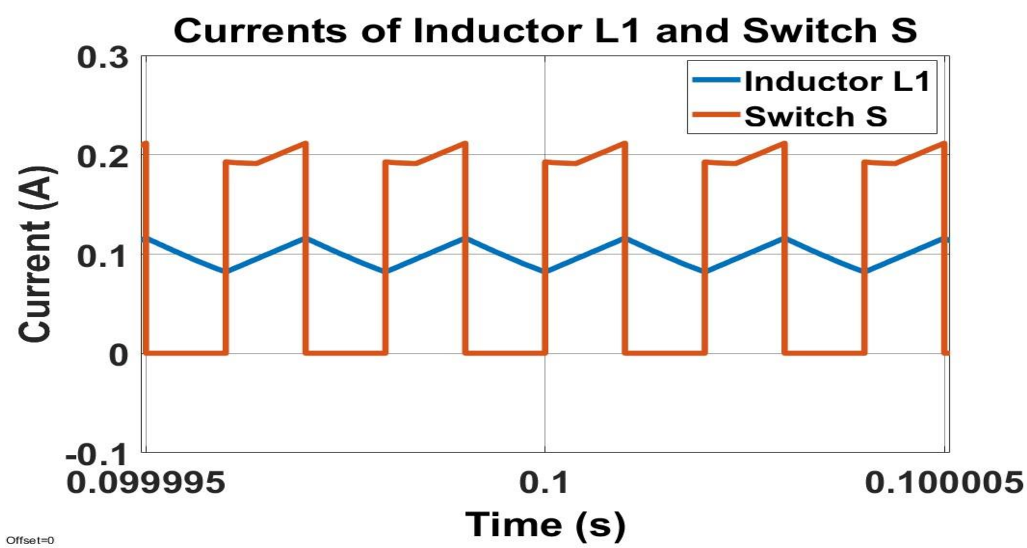


Figure (4.10). Inductor L1 and Switch S Current waveform of proposed modified POSLLC at D=0.5.

Figure (4.11) shows the inductor LI 's voltage and current waveform. According to the equations, this inductor's highest and lowest voltages alternated between 12 and 12 VDC. This graph attests to the voltage's alignment with the predicted values. The pattern of waves seen in Figure (4.11) is mirrored in the present waveform.

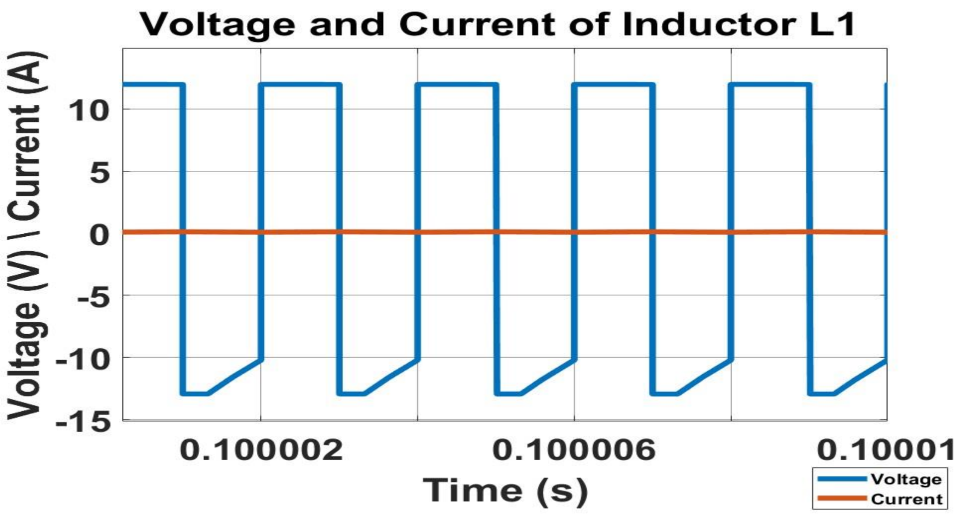


Figure (4.11). Inductor L1 voltage and current of proposed modified POSLLC

The input and output power of the converter are shown in Figure (4.12). The average input current is roughly 20 times higher than the expected output current . One practical solution to reduce the current ripple is to use larger inductors.

Moreover, reducing the diodes' switching losses is essential to improving efficiency. More accurate soft-switching methods, like zero switching or zero transition approaches, can accomplish this. These sophisticated techniques can reduce switching-related losses, enhance the agreement between theoretical and mathematical analysis, and ultimately maximize the effectiveness of the suggested topology.

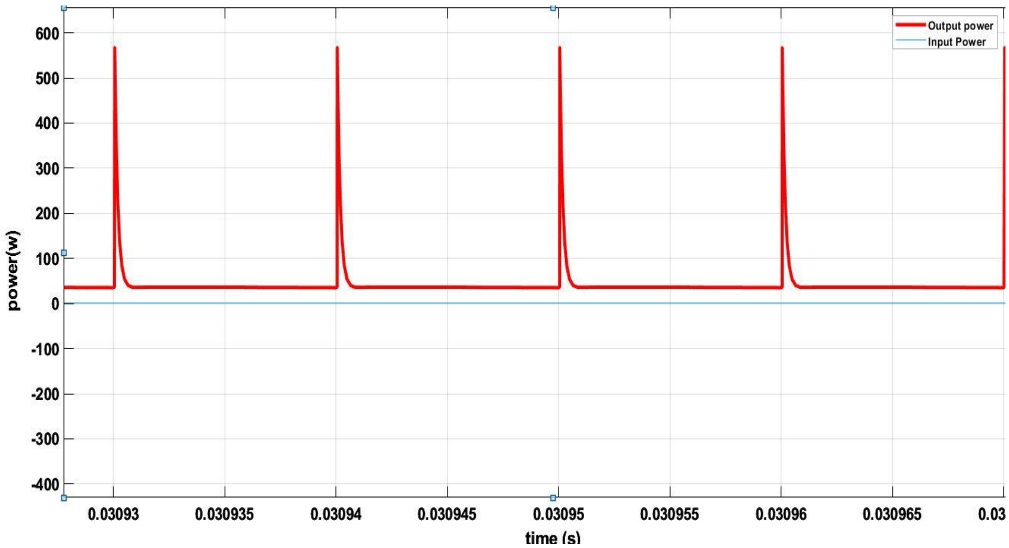


Figure (4.12). The input and output power of the proposed modified converter

Figure (4.13) shows the percentages of losses across the converter's constituent parts. Significantly, diodes were shown to be the primary cause of losses. Fast and low-power diodes can mitigate such losses. Moreover, including an appropriate snubber circuit was considered advantageous, mainly when soft switching minimizes switching losses. Furthermore, switching losses suffered by the switch can be effectively minimized by using power switches of a similar kind and an identical soft switching paradigm.

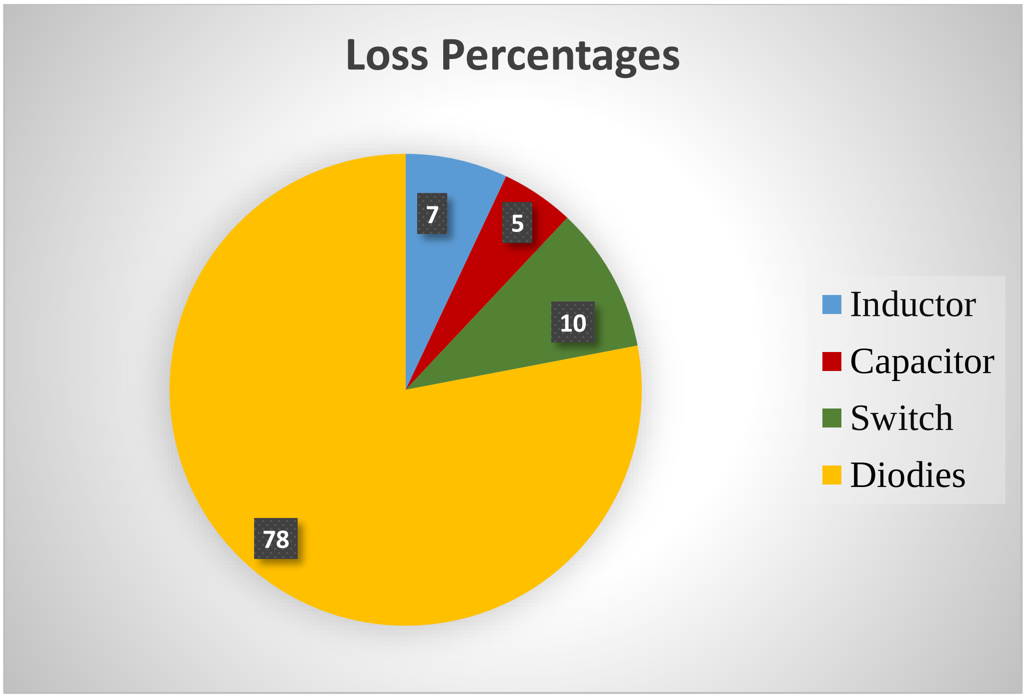


Figure (4.13). The loss percentages in the components of the proposed modified converter

4.3 Simulation Results for Multistage Switched Capacitor Technique

By employing the MSCC approach, simulating the POSLLC yields valuable insights into its performance under different operating situations. Simulation studies are extremely helpful for comprehending the dynamic behavior of the converter, improving its design parameters, and forecasting its performance in real-world scenarios.

In figure (4.14) the output voltage of the conventional positive output super lift Luo converter with respect to the input voltage shows the simple amplification in voltage. figure (4.15) illustrates the output voltage of proposed modified POSLLC at duty cycle = 0.5 with respect to the input voltage. While figure (4.16) shows the output voltage of the proposed modified POSLLC using a multi switched capacitor cell at duty cycle =0.5.

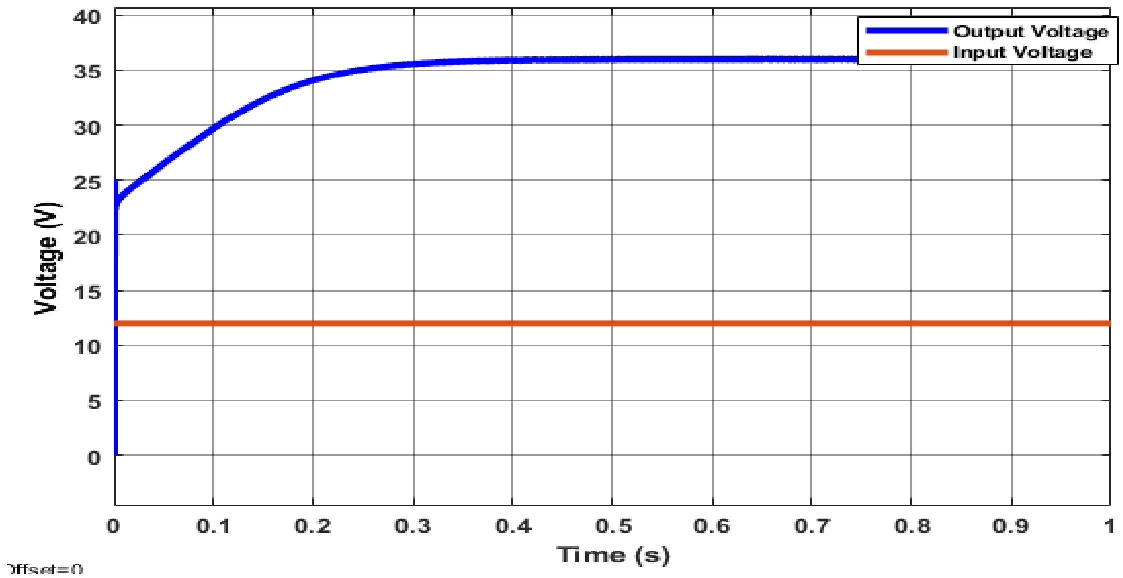


Figure (4.14). Input &Output voltage of conventional POSLLC at K=0.5

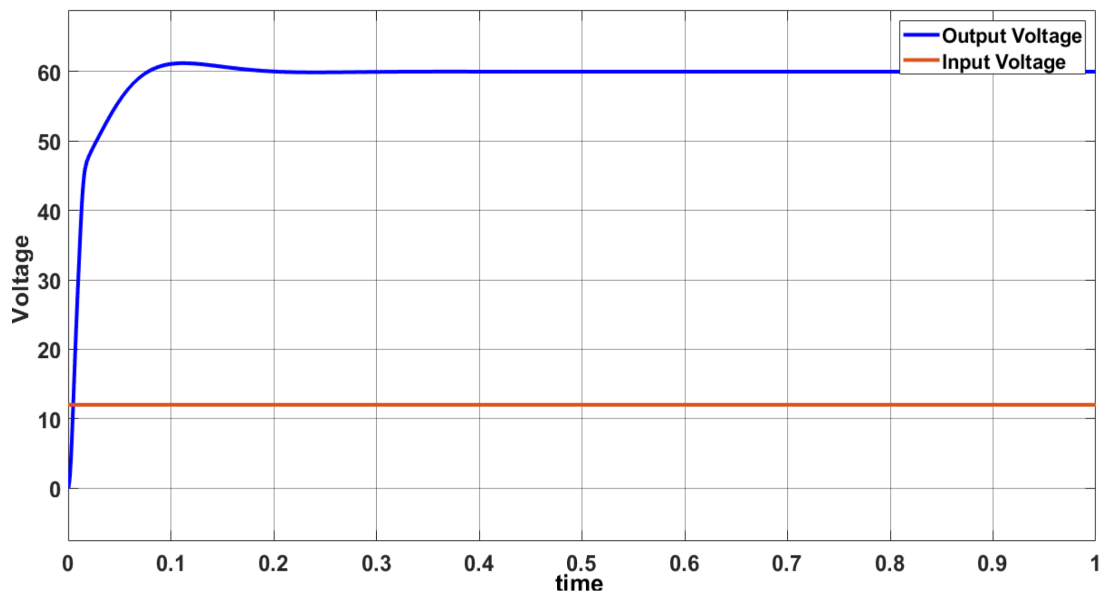


Figure (4.15). Input & Output voltage of modified switched capacitor cell at K=0.5

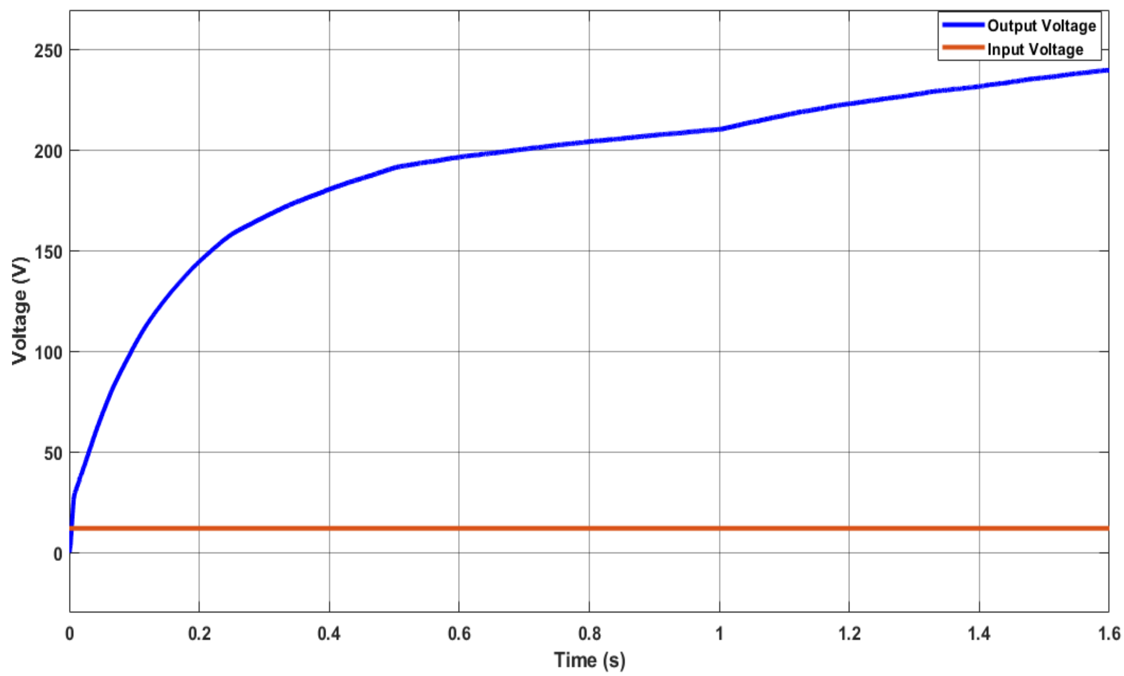


Figure (4.16). Input & Output voltage of multi switched capacitor cell at K=0.5

4.4 Comparative Analysis

This part aims to make comparing the many boost converter models reported recently easier. The objective is to evaluate the proposed converter's position relative to its competitors. These converters should be carefully examined in several areas, including the number of parts (inductors, diodes, capacitors, and transistors), the voltage amplification, the voltage stress, their overall efficiency, the voltage stresses, and the complexity of the control strategies used to guarantee an output voltage that is constant for the attached load.

when the duty cycle was K=0.5 , the results obtained in three cases are shown in the table (4.1) below:

i) Conventional POSLLC .
ii) Proposed modified POSLLC with a switched capacitor cell .
iii) Proposed modified POSLLC with a multi-switched capacitor cell .

In table 4.1. it can be noticed that the value of transfer voltage gain in the proposed modified POSLLC with multi-switched capacitor cell is twenty times the gain value in the conventional POSLLC .

The double cell stage configuration offers a notable increase in output voltage and gain, and increased component count. However, it requires a more complicated design with a higher number of components. The selection of the suitable configuration is contingent upon the particular demands of the application, such as the trade-offs between higher voltage gain and complexity.

Table 4.1 : Summarized the simulation results of proposed POSLLC at K=0.5

Parameter	**Conventional POSLLC**	**Modified POSLLC with s.c cell**	**Modified POSLLC with multi s.c cell**
Vin	12V	12V	12V
Vo	36 V	60 V	240V
Gain	3	5	20
Ripple factor	0.12	0.15	0.6
No. of components	6	12	19

The proposed converter uses just one power switch. By accepting different loads and supply sources. Furthermore, the proposed converter's gain equation shows how much better it is than other converters regarding voltage amplification.

The proposed converter demonstrated noteworthy benefits and features while considering the different converter configurations and the complexities associated with the control mechanism. For instance, the single power switch in the converter's construction was designed to reduce the circuit's switching and dynamic losses. In addition, by eliminating the need for complex separate switching circuits, this configuration expedited the control mechanism and reduced possible difficulties during real-world deployments. In table (4.2) shows a comparison of proposed converter and other boost converters.

Table (4.2): Comparison of proposed and other boost converters.

Technique	Component	Voltage Gain	Voltage Stress Switch
[110]	16	$\frac{5-K}{1-K}$	$\frac{2}{1-K}Vo$
[111]	14	$\frac{1+K}{1-K}$	$\frac{1+K}{1-K}V_o$
[112]	8	$\frac{1+K}{1-K}$	–
[113]	7	$\frac{1}{(1-K)}$	–
[107]	8	$\frac{1+K}{1-K}$	$\frac{1}{1-K}V_{in}$
[114]	8	$\frac{1}{(1-K)}$	–
[115]	7	$\frac{1-K}{1-2K}$	$\frac{1}{1-K}V_{in}$
[34]	12	$\frac{4}{1-K}$	–
[10]	9	$\frac{2}{1-K}$	–
Proposed	19	$\frac{12-4K}{1-K}$	$\frac{1}{1-K}V_{in}$

The converter also showed ripples at low input current. This was explained by the circuit's inductors charged in parallel and discharged in series. The ensuing short input current ripple extended the supplied source's lifetime, especially when high-frequency switching was an issue .

In Table 4.3, The proposed converter demonstrates exceptional performance with its simple design utilizing a multi-switched capacitor cell, achieving a high voltage gain of 20, stepping up 12 V to 240 V . The proposed converter's high gain make it a superior choice for compact, high step-up applications

Table (4.3) : Comparison between the Proposed Converter and Previous work DC- DC Converters.

Items	The proposed converter	**[34]**	**[116]**	**[117]**	**[118]**	**[39]**	**[43]**
F_S (kHz)	100	150	50	24	45	50	50
Vin	12	20	20	20	20	65	12
Vo	240	200	200	300	155	500	96
L	3	4	5	2	2	2	4
C	8	4	8	4	8	2	4
Diode	7	1	4	4	7	2	9
Switch	1	1	1	1	1	1	1
Duty cycle	50 %	45%	60%	77%	77%	55%	55%
Gain	20	10	10	15	8	8	8

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CHAPTER FIVE

Chapter Five
Conclusions and Future Work

5.1 Conclusions.

A positive output super lift Luo converter with switched-capacitor cell is proposed. The proposed modified POSLLC circuit was designed ,analyzed and compared with the conventional POSLLC circuit. Moreover ,a multi-switched capacitor cell at the output was added to enhance the performance of the proposed system and the following conclusions were obtained:

1. A duty cycle and various operational modes were applied together with a mathematical analysis to produce a voltage approaching 250 VDC at the converter's output side, For K=0.5, 12 VDC was set as input voltage a simulated output voltage of 60 VDC was obtained.
2. The proposed converter, which had a single power switch, reduced switching, and dynamic losses, simplified the control procedure. Its competitive advantage over options with several power diodes stemmed from its cost-effectiveness, demonstrated by decreased overall expenses for a single power switch. Because of its higher voltage gain, the converter was especially suitable for low-voltage supply uses, such as solar panels.
3. It significantly reduced input current ripples, extending input supply life in high-frequency switching circumstances.
4. It utilized a multistage switched capacitor cell technique to improve the transfer voltage gain and overall performance of the modified positive output super lift Luo converter achieving simulated output voltage of 240 VDC at K =0.5 and transfer voltage gain 20 times with input voltage was set to 12 VDC . The technique improved transfer voltage gain, reduced stress on switching devices and capacitors. It was compatible with low voltage applications.

5.2 Recommendations for Future work

There are several points for future research and development that can gives more enhancement for the design and expands its effectiveness :

1. For future work could design and implement a prototype circuit for the Modified Positive Output Super Lift Luo Converter so that the simulation results in the current thesis may be compared to the experimental results obtained.
2. Despite that the multi-stage switched capacitor cell technique demonstrate a promising results, there is a potential further optimization . for future research could try a new configuration of (MSCC) or switching strategies or control algorithms to accomplish a higher gain and efficiency .
3. Proposed modified converter can be tested to be used in renewable energy application, Future research could consternate on optimizing the converter to overcome obstacles associated with input voltage ripple and assuring consistent operation in a broader spectrum of circumstances.

REFERENCES

References

[1] Forouzesh, M., Siwakoti, Y.P., Gorji, S.A., Blaabjerg, F. and Lehman, B. (2017). Step-Up DC–DC Converters: A Comprehensive Review of Voltage-Boosting Techniques, Topologies, and Applications. *IEEE Transactions on Power Electronics*, 32(12), pp.9143–9178. doi:https://doi.org/10.1109/tpel.2017.2652318.

[2] M. Chen, C. Yin, P. C. Loh and A. Ioinovici, "Improved Large DC Gain Converters with Low Voltage Stress on Switches Based on Coupled-Inductor and Voltage Multiplier for Renewable Energy Applications," In *IEEE Journal of Emerging and Selected Topics in Power Electronics* 2019.

[3] Malik, M.Z.; Xu, Q.; Farooq, A.; Chen, G. A new modified quadratic boost converter with high voltage gain. IEICE Electron. Express 2017.

[4] A. Ho, T. Chun and H. Kim, "Extended Boost Active-Switched Capacitor/Switched-Inductor Quasi-Z-Source Inverters," In *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5681-5690, Oct. 2015.

[5] X. Zhu, B. Zhang, Z. Li, H. Li and L. Ran, "Extended Switched-Boost DC-DC Converters Adopting Switched-Capacitor/Switched-Inductor Cells for High Step-up Conversion," In IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 3, pp. 1020-1030, Sept. 2017.

[6] M. Zhu, T. Wang and F. L. Luo, "Analysis of voltage-lift-type boost converters," IEEE Conference on Industrial Electronics and Applications (ICIEA), pp. 214-219, Singapore, 2012.

[7] Y. Hsieh, J. Chen, T. Liang and L. Yang, "Novel High Step-Up DC–DC Converter for Distributed Generation System," In *IEEE Transactions on Industrial Electronics*, vol. 60, no. 4, pp. 1473-1482, April 2013.

[8] F. M. Shahir, E. Babaei and M. Farsadi, "Extended Topology for a Boost DC– DC Converter," In IEEE Transactions on Power Electronics, vol. 34, no. 3, pp. 2375-2384, March 2019.

[9] B. Axelrod, Y. Berkovich and A. Ioinovici, "Transformerless DC-DC converters with a very high DC line-to-load voltage ratio," Proceedings of the 2003 International Symposium on Circuits and Systems, ISCAS '03., Bangkok, 2003.

[10] Luo, F.L.; Ye, H. Advanced DC-DC Converters; CRC Press: Boca Raton, FL, USA, 2016.

[11] Fang Lin Luo. Investigation on Split-inductors applied in positive output Super-Lift Luo-Converters. 2011 May 1;

[12] Jose J, B Jayanand. Simulation and implementation of superlift Luo converter. 2013 Dec 1;

[13] A.Manikandan, N.Vadivel . Design And Implementation Of Luo Converter For Electric Vehicle Application. International Journal of Engineering Trends and Technology (IJETT) – Volume 4 Issue 10 - Oct 2013
[14] Jayachandran DN, Krishnaswamy V, Anbazhagan L, Dhandapani K. Modelling and Analysis of Voltage Mode Controlled Luo Converter. American Journal of Applied Sciences. 2015 Oct 1;12(10):766–74.
[15] Bright SJV, Ramkumar S, Anand H. Positive output elementary Luo converter for fixed-frequency ZVS operation. Bulletin of the Polish Academy of Sciences Technical Sciences. 2017 Apr 1;65(2):255–62.
[16] S.Usha, C.Subramani, R.Muthulakshmi, R.Ramya, R.Kaveri, Harshit Singh. Positive Output Elementary Super Lift Luo Converter Using Pi Controller. International Journal of Recent Technology and Engineering. 2019 Nov 2;8(2S11):3406–10.
[17] Adlakha R, Khosla A, Joshi D. Comparative analysis of positive output super lift DC-DC luo converters. Indonesian Journal of Electrical Engineering and Computer Science. 2020 May 1;18(2):707.
[18] S. Usha, A. Geetha, T. M. Thamizh Thentral, R. Muthulakshmi, T. Manju, R. Kaveri. Performance Analysis of Luo and Modified Luo Converter Using Soft Switching Technique. Social Science Research Network. 2020 Jan 1;
[19] Gholizadeh H, Sharifi Shahrivar R, Hashemi M, Afjei E, A. Gorji S. Design and Implementation a Single-Switch Step-Up DC-DC Converter Based on Cascaded Boost and Luo Converters. Energies. 2021 Jun 16;14(12):3584.
[20] Ghasemi F, Yazdani MR, Delshad M. Step-Up DC-DC Switching Converter With Single Switch and Multi-Outputs Based on Luo Topology. IEEE Access. 2022;10:16871–82.
[21] Rudenko Y. Analysis of DC-DC volt-inverting Luo converter with reduced output voltage ripples operating in DCM. 2023 Oct 2;
[22] G. Bharani, M. Elango, U. Harshavarshini, G. Karthick, S. Dineshkumar. Design And Implementation Of Luo Converter For Renewable Application. 2023 Mar 23;
[23] Hsieh YP, Chen JF, Liang TJ, Yang LS. Novel High Step-Up DC–DC Converter With Coupled-Inductor and Switched-Capacitor Techniques. IEEE Transactions on Industrial Electronics. 2012 Feb;59(2):998–1007.
[24] Luo FL, Ye H. Hybrid split capacitors and split inductors applied in positive output super-lift Luo-converters. IET Power Electronics. 2013 Nov 1;6(9):1759–68.

[25] Bahrami H, Iman-Eini H, Kazemi B, Taheri A. Modified step-up boost converter with coupled-inductor and super-lift techniques. IET Power Electronics. 2015 Jun;8(6):898–905.
[26] Abid R, Ferdaous Masmoudi, Nabil Derbel. Comparative study of the performances of the DC/DC luo-converter in photovoltaic applications. 2017 Feb 1;
[27] Yang LS. Implementation of high step-up DC-DC converter using voltage-lift and coupled inductor techniques. International Journal of Circuit Theory and Applications. 2018 Jun 4;46(11):2079–97.
[28] Tekade AS, Juneja R, Kurwale MV, Prashant Debre. Design of Positive Output Super-Lift Luo Boost Converter for Solar Inverter. 2019 Apr 1;
[29] Hamid Khudair Khalil, Saad S. Hreshee, Hassan Jassim Motlak. Design and Implementation of Photovoltaic System Based on Super-Lift LUO Converter. Journal of Physics: Conference Series 2020, doi:10.1088/1742-6596/1530/1/012013
[30] Zhang X, Sun L, Guan Y, Han S, Cai H, Wang Y, et al. Novel High Step-Up Soft-Switching DC–DC Converter Based on Switched Capacitor and Coupled Inductor. IEEE Transactions on Power Electronics. 2020 Sep;35(9):9471–81.
[31] Mohammed, Ahmed T., and Nabil K. Alshamaa. "Design and implementation of a modified Luo converter with higher–voltage ratio gain." IOP Conference Series: Materials Science and Engineering. Vol. 881. No. 1. IOP Publishing, 2020.
[32] Rahimi, Tohid, et al. "An ultra high step-up DC–DC converter based on the boost, luo, and voltage doubler structure: mathematical expression, simulation, and experimental." IEEE Access 9 (2021): 132011-132024.
[33] Jassim, Ream Mohammed, Kadhim H. Hassan, and Issa Ahmed Abed. "Comparison between boost and positive output super lift Luo converters to improve the performance of photovoltaic system." Bulletin of Electrical Engineering and Informatics 11.5 (2022): 2479-2490.
[34] Hussein HAK, Motlak HJ. Improving the design of super-lift Luo converter using hybrid switching capacitor-inductor cell for PV system. Indonesian Journal of Electrical Engineering and Computer Science. 2022 Feb 1;25(2):710
[35] Hussein Abdulkhudhur Hussein, Hassan Jassim Motlak, Abdali N. Effect of switched-capacitor on super-lift Luo converter. Bulletin of Electrical Engineering and Informatics. 2022 Dec 1;11(6):3119–26.
[36] Gholizadeh, Hossein, and Lazhar Ben-Brahim. "A new non-isolated high-gain single-switch DC–DC converter topology with a continuous input current." Electronics 11.18 (2022): 2900.

[37]Ghafour ZA, Ajel AR, Yasin NM, Noaman Mohammad Noaman. Efficient Design, Analysis and Implementation of Super-Lift LUO Converter for Standalone PV Applications. Journal of techniques. 2023 Jun 24;5(2):81–8.
[38]Ammar Falah Algamluoli, Wu X. A New Single-Cell Hybrid Inductor-Capacitor DC-DC Converter for Ultra-High Voltage Gain in Renewable Energy Applications. Electronics. 2023 Jul 17;12(14):3101–1.
[39] Aseela Sweatha, Baskaran B, P. Duraipandy. A novel voltage lifting technique of switched-inductor cell based modified LUO converter topology for water pumping system. International Journal of Applied Power Engineering. 2023 Dec 1;12(4):416–6.
[40] Kumar M, Vinod Kumar Yadav, Kirti Mathuria, Arun Kumar Verma. A Soft Switched High Gain Boost Converter With Coupled Inductor for Photovoltaic Applications. IEEE journal of emerging and selected topics in industrial electronics. 2023 Jul 1;4(3):827–35.
[41] Kumar M, Vinod Kumar Yadav, Arun Kumar Verma. Switched Capacitor Based High Gain Boost Converter for Renewable Energy Application. IEEE journal of emerging and selected topics in industrial electronics. 2023 Jul 1;4(3):818–26.
[42] K. Ramash Kumar, S. Jeevananthan. PI Control for Positive Output Elementary Super Lift Luo Converter. International Journal of Electrical and Computer Engineering. 2010 Mar 23;4(3):544–9.
[43]Kumar KR, Jeevananthan S. Sliding Mode Control for Current Distribution Control in Paralleled Positive Output Elementary Super Lift Luo Converters. Journal of Power Electronics. 2011 Sep 20;11(5):639–54.
[44]N. Arunkumar, Sivakumaran TS, K. Ramash Kumar, S. Saranya, Swaroop Memorial. REDUCED ORDER LINEAR QUADRATIC REGULATOR PLUS PROPORTIONAL DOUBLE INTEGRAL BASED CONTROLLER FOR A POSITIVE OUTPUT ELEMENTARY SUPER LIFT LUO-CONVERTER. 2014 Jan 1;
[45] K. Ramash Kumar, S. Jeevananthan, S. Ramamurthy. Improved Performance of the Positive Output Elementary Split Inductor-Type Boost Converter using Sliding Mode Controller plus Fuzzy Logic Controller.2014
[46] Siddharthan N, Balasubramanian B. Performance evaluation of SEPIC, Luo and ZETA converter. International Journal of Power Electronics and Drive Systems (IJPEDS). 2019 Mar 1;10(1):374.
[47] Malek Guizani, Abid R, Ferdaous Masmoudi, Djemel M, Nabil Derbel. the Performance Analysis of DC-DC Luo-Converter for Photovoltaic Application. 2018 Mar 1:756-761.

[48] Nath S, Jayarama Pradeep. PV based design of improved positive output super-lift Luo converter. 2016 Mar 1;
[49] S. Vijai Ananth, S. Singaravelu. Modelling and Simulation of MPPT Based Solar Photovoltaic System for Voltage Lift LUO Converter. International journal of electrical & electronics research. 2023 Mar 30;11(1):90–6.
[50] Nazrin Salma S, Dhanalakshmi S, Rajkumar M. Design and Control of Modified Super Lift Luo Converter for Electric Vehicle Applications. Electric Power Components and Systems. 2023 Apr 17;1–12.
[51] Amit Kumar, Sushil Kumar "Designing and Developing DC-DC Converter using Various Controller: A Comprehensive Review " in Compliance Engineering Journal, Volume 14, Issue 10, 2023.
[52] B. Axelrod, Y. Berkovich, S. Tapuchi, A. loinovici, "Steep conversion ration Ćuk, Zeta, and Sepic converters based on a switched coupled-inductor cell," In 2008 IEEE Power Electronics Specialists Conference, pp. 3009-3014. June 2008.
[53] N. Bajoria, P. Sahu, R. K. Nema and S. Nema, "Overview of different control schemes used for controlling of DC-DC converters," 2016 Int. Conf. on Elect. Power and Energy Systems (ICEPES), Bhopal, pp. 75-82, 2016
[54] R. Basak, P. Nishita, Z. Elias, S. Sreejith, "High gain Boost Converter with reduced switching stress," 2015 Int. Conf. on Computation of Power, Energy, Information and Communication (ICCPEIC), Chennai, 2015, pp. 0393-0399.
[55] Ping Yang, Jianping Xu, Guohua Zhou and Shiyu Zhang, "A new quadratic boost converter with high voltage step-up ratio and reduced voltage stress," Proc. of The 7th Int. Power Electronics and Motion Control Conf., Harbin,, pp. 1164-1168, 2012.
[56] Lithesh, Gottapu, Bekkam Krishna, and V. Karthikeyan. "Review and comparative study of bi-directional DC-DC converters." 2021 IEEE International Power and Renewable Energy Conference (IPRECON). IEEE, 2021.
[57] Yi, Feilong, and Faqiang Wang. "Review of voltage-bucking/boosting techniques, topologies, and applications." Energies 16.2 (2023): 842.
[58] Vishnuram, Pradeep, et al. "A comprehensive review on EV power converter topologies charger types infrastructure and communication techniques." Frontiers in Energy Research 11 (2023): 1103093.
[59] Sutikno, Tole, Rizky Ajie Aprilianto, and Hendril Satrian Purnama. "Application of non-isolated bidirectional DC–DC converters for renewable

and sustainable energy systems: a review." Clean Energy 7.2 (2023): 293-311.
[60] Afonso, Joao L., et al. "A review on power electronics technologies for power quality improvement." Energies 14.24 (2021): 8585.
[61] Raghavendra, Kummara Venkat Guru, et al. "A comprehensive review of DC–DC converter topologies and modulation strategies with recent advances in solar photovoltaic systems." electronics 9.1 (2019): 31.
[62] Kolli, Abdelfatah, et al. "A review on DC/DC converter architectures for power fuel cell applications." Energy Conversion and Management 105 (2015): 716-730.
[63] Gopi, R. Reshma, and S. Sreejith. "Converter topologies in photovoltaic applications–A review." Renewable and Sustainable Energy Reviews 94 (2018): 1-14.
[64] Habib, Salman, et al. "Contemporary trends in power electronics converters for charging solutions of electric vehicles." CSEE Journal of Power and Energy Systems 6.4 (2020): 911-929.
[65] Meshael, Hazem, Ahmad Elkhateb, and Robert Best. "Topologies and Design Characteristics of Isolated High Step-Up DC–DC Converters for Photovoltaic Systems." Electronics 12.18 (2023): 3913.
[66] Kouro, Samir, et al. "Recent advances and industrial applications of multilevel converters." IEEE Transactions on industrial electronics 57.8 (2010): 2553-2580.
[67] Mumtaz, Farhan, et al. "Review on non-isolated DC-DC converters and their control techniques for renewable energy applications." Ain Shams Engineering Journal 12.4 (2021): 3747-3763.
[68] Femi, R., T. Sree Renga Raja, and R. Shenbagalakshmi. "A positive output-super lift Luo converter fed brushless DC motor drive using alternative energy sources." International Transactions on Electrical Energy Systems 31.2 (2021): e12740.
[69] Venugopal, R., et al. "Review on unidirectional non-isolated high gain DC-DC converters for EV sustainable DC fast charging applications." IEEE Access (2023).
[70] Shahzad, Danish, et al. "A high-power-density high-efficiency soft-switched single-phase universal input to 28-V isolated AC–DC converter module designed for paralleled operation." IEEE Transactions on Power Electronics 37.7 (2022): 8262-8280.
[71] Navamani, J. Divya, et al. "Modified LUO high gain DC-DC converter with minimal capacitor stress for electric vehicle application." IEEE Access 9 (2021): 122335-122350.

[72] F. Mohammad zadeh Shahir, E. Babaei and M. Farsadi, "Voltage-Lift Technique Based Non isolated Boost DC-DC Converter: Analysis and Design," In IEEE Trans. on Power Electronics, vol. 33, no. 7, pp. 5917-5926, July 2018.
[73] S. Y. Kim, et al., "Design of a high efficiency DC-DC buck converter with two- step digital PWM and low power self-tracking zero current detector for IoT applications," IEEE Transactions on Power Electronics, 33(2), 1428-1439, 2017.
[74] J. Sreedhar, B. Basavaraju, "Design and analysis of synchronous buck converter for UPS application," 2016 2nd Int. Conf. on Adv. in Elect. Electronics, Inf.Commun. and Bio-Informatics (AEEJCB), Chennai, pp. 573-579, 2016.
[75] M.M. Garg, Y. V. Hote, M.K. Pathak, "Design and Performance Analysis of a PWM DC-DC Buck Converter Using PI Lead Compensator," Arabian Journal for Science and Engineering, vol. 40, no. 12, pp. 3607-3626, 2015.
[76] T. Salvatierra, M.K. Kazimierczuk, "DC analysis and design of a PWM buck converter operated as a dynamic power supply," International Journal of Circuit Theory and Applications, vol. 45, no. 5, pp. 681-706, 2016.
[77] Z. Li, K. W. E. Cheng and J. Hu, "Modelling of basic DC-DC converters," 2017 7th Int. Conf on Power Flectronics Systems and Applications - Smart Mobility Parth Transfer & Security (PESA), Hong Kong, pp. 1-8, 2017.
[78] S. Chander, P. Agarwal and I. Gupta, "Design, modeling and simulation of DC-DC converter," 2010 Conf Proc. IPEC, Singapore, 2010, pp. 456-461.
[79] S. Vavilapalli, S. Umashankar, P. Sanjeevikumar, V. Fedák, L. Mihet-Popa, V. K. Ramachandaramurthy, "A buck-chopper based energy storage system for the cascaded 11-bridge înverters in PV applications," Energy Procedia, vol. 145, pp. 534-541, 2018.
[80] B. M. Hasaneen and A. A. Elbaset Mohammed, "Design and simulation of DC-DC boost converter," 2008 12th International Middle-East Power System Conference, Aswan, pp. 335-340, 2008.
[81] S. Masri and P. W. Chan, "Design and development of a DC-DC boost converter with constant output voltage," 2010 International Conference on Intelligent and Advanced Systems, Manila, pp. 1-4, 2010.
[82] B. J. Saharia, M. Manas and S. Sen, "Comparative Study on Buck and Buck- Boost DC-DC Converters for MPP Tracking for Photovoltaic Power Systems," 2016 Second International Conference on Computational Intelligence & Communication Technology (CICT), Ghaziabad, pp. 382-387, 2016.

[83] B. R. Kiran and G. A. Ezhilarasi, "Design and analysis of soft-switched Buck-Boost Converter for PV applications," 2015 Annual IEEE India Conference (INDICON), New Delhi, pp. 1-5, 2015.
[84] S. S. Alharbi, S. S. Alharbi, A. M. S. Al-bayati and M. Matin, "Design and performance evaluation of a DC-DC buck-boost converter with cascode GaN FET, SIC JFET, and Si IGBT power devices," 2017 North American Power Symposium (NAPS), Morgantown, WV, 2017.
[85] Lovepreet Kaur Grewal and Navdeep Kaur Brar, Analysis, Design and Simulation of DC-DC Boost Converter (2016
[86] Aaron Yong, MPhil Engineering, University of Cambridge (2018)
[87] Usharani, V., and R. Agasthiya. "Enhanced MPPT Technique For DC-DC Luo Converter Using Model Predictive Control For Photovoltaic Systems." International Journal of Engineering Research and Development 11.01 (2015).
[88] Silpa. N and Chitra. J , "An Improved Luo Converter for High Voltage Applications ", International Journal of Emerging Technology and Advanced Engineering, Volume 4, Issue 5, May 2014.
[89] Fang Lin Luo and Hong Ye, "Super-lift Boost Converter", IET Power Electron, Vol. 7, Issue 7, 2014.
[90] Zhu, Miao, Tao Wang, and Fang Lin Luo. "Analysis of voltage-lift-type boost converters." 2012 7th IEEE Conference on Industrial Electronics and Applications (ICIEA). IEEE, 2012.
[90] Luo, Fang Lin. "Luo-converters, voltage lift technique." PESC 98 Record. 29th Annual IEEE Power Electronics Specialists Conference (Cat. No. 98CH36196). Vol. 2. IEEE, 1998.`
[92] Luo, Fang Lin, Hong Ye, and M. H. Rashid. "Super-lift Luo-converters." 2002 IEEE 33rd Annual IEEE Power Electronics Specialists Conference. Proceedings (Cat. No. 02CH37289). Vol. 2. IEEE, 2002.
[93] Muhammad H. Rashid, "Power Electronics Handbook, Device, Circuit and Applications", Third Edition, 2011.
[94] R.Venugopal, M. Prabu, DESIGN AND DEVELOPMENT OF POSITIVE OUTPUT SUPER-LIFT CONVERTER USING PROTEUS SOFTWARE.
[95] van der Horst Bruyn, Jon. "Applications of LUO Converters." University of Auckland, Department of Electrical Engineering Part IV Project Final Report (2004).
[96] Luo, F. L., and H. Ye. "Negative output super-lift Luo-converters." IEEE 34th Annual Conference on Power Electronics Specialist, 2003. PESC'03.. Vol. 3. IEEE, 2003.

[97] F. L. Luo, H. Ye, and M. H. Rashid, “Multiple-quadrant Luo converters,”Proc. Inst. Elect. Eng., vol. 148, no. 1, pp. 9–18, Jan. 2002.
[98] R.Suguna, A.Mutharasan, PV FED BY NEGATIVE OUTPUT SUPER-LIFT LUO CONVERTER USING IMPROVED P&O MPPT (2017).
[99] Afroz Pasha and N.Jayakumar, Design And Simulation of INC MPPT Based Super Lift -Luo Boost Converter For Solar Pv Applications.
[100] Dhas, G. Justin Sunil, D. Anto Sahaya Dhas, and M. K. Sreesna. "Positive Output Elementary Superlift Luo Converter for PV Applications." 3rd International conference on Innovative Engineering Technologies. 2016.
[101] Luo, Fang Lin, and Hong Ye. "Positive output super-lift converters." IEEE Transactions on Power Electronics 18.1 (2003): 105-113.
[102] Balaji, B., and J. Barnabas Paul Glady. "Simulation and fault diagnosis of positive output elementary super lift Luo converter." ARPN Journal of Engineering and Applied Sciences (2006).
[103] Shalini, K., and J. Barnabas Paul Glady. "Solar Powered Luo Converter for Wiper Motor Application." Indian Journal of Science and Technology 9.43 (2016).
[104] Fang Lin Luo. Investigation on Split-Capacitors applied in positive output Super-Lift Luo-Converters. 2011 May 1: 2792–2797
[105] J. Saharia, M. Manas and S. Sen, "Comparative Study on Buck and Buck-Boost DC-DC Converters for MPP Tracking for Photovoltaic Power Systems," 2016 Second international Conference on Computational Intelligence & Communication Technology CICT), Ghaziabad, pp. 382-387, 2016.
[106] D. Jahanbakhsh, "Implementation of DC-DC converter with maximum power point ding control for thermoelectric generator applications," Stockholm: Royal Institute Technology (KTH), 2012.
[107] B. Axelrod, Y. Berkovich and A. loinovici, "Switched-capacitor (SC)/switched inductor (SL) structures for getting hybrid step-down Cuk/Sepic/Zeta converters," 2006 IEEE International Symposium on Circuits and Systems, Island of Kos, pp. 5063-5066, 2006.
[108] M. Chen, K. Li, J. Hu, A. loinovici "Generation of a Family of Very High DC Gain Power Electronics Circuits Based on Switched-Capacitor-Inductor Cells Starting from Simple Graph," IEEE Transactions on Circuits and Systems 1. Regular Papers, vol.63, пo.12, pp. 2381-2392, 2016.
[109] Berkovich Y, Axelrod B, Madar R, Avraham Twina. Improved Luo converter modifications with increasing voltage ratio. Iet Power Electronics. 2015 Feb 1;8(2):202–12.

[110] Davut Ertekin, Kübra Baltacı, Mehmet Çelebi. Advancing Renewable Energy: An Experimental Study of a Switched-Inductor, Switched-Capacitor Luo Boost Converter for Low-Voltage Applications. Electronics. 2023 Dec 14;12(24):5006–6.
[111] Abbasi, Maysam, Ehsan Abbasi, and Li Li. "New transformer-less DC–DC converter topologies with reduced voltage stress on capacitors and increased voltage conversion ratio." IET Power Electronics 14.6 (2021): 1173-1192.
[112] Saravanan, Subramani, and Neelakandan Ramesh Babu. "A modified high step-up non-isolated DC-DC converter for PV application." Journal of applied research and technology 15.3 (2017): 242-249.
[113] Oluwafemi, Adepoju Webster, et al. "A modified high output-gain cuk converter circuit configuration for renewable applications—A comprehensive investigation." 2017 IEEE Conference on Energy Conversion (CENCON). IEEE, 2017.
[114] Muranda, Charles, et al. "Modified SEPIC DC-to-DC boost converter with high output-gain configuration for renewable applications." 2017 IEEE Conference on Energy Conversion (CENCON). IEEE, 2017.
[115] Patidar, Keshav, and Amod C. Umarikar. "A step-up PWM DC–DC converter for renewable energy applications." International Journal of Circuit Theory and Applications 44.4 (2016): 817-832.
[116] Rajesh, R.; Prabaharan, N. Design of New Nonisolated High Gain Converter for Higher Power Density. Int. Trans. Electr. Energy Syst. 2023, 2011926.
[117] Saravanan, S.; Babu, N.R. Design and Development of Single Switch High Step-Up DC–DC Converter. IEEE J. Emerg. Sel. Top. Power Electron. 2017, 6, 855–863.
[118] Hassani, M.Y.; Maalandish, M.; Hosseini, S.H. A Single-Switch High Step-Up DC–DC Converter with Low Input Current Ripple for Renewable Energy Applications. In Proceedings of the 2022 13th Power Electronics, Drive Systems, and Technologies Conference (PEDSTC), Tehran, Iran, 1–3 February 2022; pp. 186–190**.**
[119]Muhammed Abduljaleel Ibrahim. Performance evaluation of PI controller for positive output Luo converter. International Journal of Power Electronics and Drive Systems. 2020 Dec 1;11(4):1816–6.

الخلاصة

تُعَدُّ الوقود الأحفوري مثل الفحم والغاز والنفط مصادر طاقة فعالة، لكنها تسبب التلوث وهي محدودة. ونتيجة لذلك، يزداد التركيز على الطاقة الشمسية، مثل السيارات التي تعمل بالطاقة الشمسية وتخزين البطاريات. ومع ذلك، فإن هذه الأنظمة تنتج كهرباء بتيار مستمر(DC) ، مما يجعل توصيلها بشبكة الطاقة أكثر تحديًا.

يقدم هذا العمل تصميمًا معدلًا لدائرة مُحوِّل "لوو" لرفع الجهد الموجب (POSLLC) من نوع DC-DC، وذلك بإضافة خلية مكثف مفتاحي .(SC) تم تصميم الدائرة وتحليلها ثم مقارنتها بالمحول التقليدي لإظهار التحسينات في الأداء. تم توصيل مكثف مفتاحي متعدد في المرحلة النهائية لنظام الإخراج المقترح. تعمل خلية المكثف المتبدل على تحسين موثوقية المصدر وعمره الافتراضي، كما تحافظ على استقرار جهد الإدخال. بالإضافة إلى ذلك، توفر هذه الخلية تضخيمًا أكبر للجهد، خاصةً للتطبيقات التي تتطلب كسبًا عاليًا باستخدام مفتاح طاقة واحد فقط.

تم بناء محول POSLLC التقليدي ومحاكاته باستخدام MATLAB/SIMULINK مع ضبط دورة التشغيل عند 0.5 وجهد إدخال بقيمة 12 فولتDC ، مما أدى إلى جهد خرج 36 فولت بمعدل تضخيم ثلاث مرات ضعف جهد الإدخال. بعد ذلك، تم تصميم المحول المعدل المقترح بإضافة خلية المكثف المفتاحي ، مما أدى إلى تحقيق جهد خرج 60 فولت DC بمعدل تضخيم خمس مرات ضعف جهد الإدخال عند نفس دورة التشغيل 0.5. علاوة على ذلك، تمت إضافة خلية مكثف مفتاحي متعددة إلى الدائرة، مما أدى إلى الحصول على جهد خرج 240 فولت بمعدل تضخيم 20 ضعف جهد الإدخال عند دورة تشغيل 0.5.

يحقق المحول المقترح تحسينات كبيرة في الجهد مع أداء متميز، كما تم التحقق من صحة ذلك من خلال التحليل النظري، وتصميم الدائرة، والمحاكاة. تسهّل هذه النتائج مزيدًا من البحث في أنظمة تحويل الطاقة ذات الكسب العالي، مما يشير إلى أن نهج المكثف المتبدل المتعدد هو تقنية مناسبة لتعزيز كسب الجهد في محولاتPOSLLC .

جمهورية العراق

وزارة التعليم العالي والبحث العلمي

جامعة بابل / كلية الهندسة

كلية الهندسة الكهربائية

تصميم محول Luo بالاعتماد على تقنية المكثفات المفتاحية المتعددة

رسالة

مقدمة الى كلية الهندسة في جامعة بابل

وهي جزء من متطلبات نيل درجة الماجستير في علوم الهندسة الكهربائية/

الكترونيك

من قبل

اسماء عقيل هادي مهدي

اشراف

الاستاذ الدكتور حسن جاسم مطلك

2024 A.D ***1446 A.H***